The Level-0 Trigger Processor for the NA62 Experiment

Stefano Chiozzi (a), Enrico Gamberini (a,b), Alberto Gianoli (a), Giorgia Mila (c,d), Ilaria Neri (a,b), Ferruccio Petrucci (a), Dario Soldi (c,d)
(a) INFN, Ferrara (Italy) - (b) University of Ferrara (Italy) - (c) INFN, Torino (Italy) – (d) University of Torino (Italy)

The main purpose of the experiment NA62 at CERN-SPS is to measure the branching ratio of the (ultra) rare decay

\[ K^+ \rightarrow \pi^+ \nu \bar{\nu} \]

with a ~ 10% precision. The expected value, according to the Standard Model, is of the order of \(10^{-10}\) thus requiring a high intensity kaon beam.

This is a 75 GeV/c momentum non-separated beam composed by a 6% component of kaons, with a total rate of ~ 750 MHz. About 10% of the produced kaons decay in-flight in the fiducial volume.

The intense flux of particles requires a high-performance trigger and data acquisition system. The Level 0 (L0) trigger applies cuts to select particular event types and should be flexible to allow for requirements in later stages of the experiment.

**NA62 Trigger Levels:**
- L0: Hardware level. 10 MHz to 1 MHz. Max latency: 1 ms.
- L1: Software level. Selection from single sub-detectors information. 1 MHz to 100 kHz. Max latency: 0(1 s).
- L2: Software level. Correlation between different sub-detectors. 100 kHz to 0(kHz). Max latency: spill period 0(10 s).

**L0TP Features:**
- Data asynchronously sent from detectors to L0TP via Ethernet using UDP protocol (primitives).
- 7 Input detectors.
- Time align and match primitives with programmable masks.
- Synchronously send selected triggers to the Timing Trigger and Control (TTC) system with fixed latency for broadcasting to detectors.

L0 Trigger Processor – two different solutions

**FPGA-based L0TP**
- L0-Trigger selection directly on the FPGA.
- Fully real-time processing with constant latency.
- Trigger matching algorithms embedded in firmware.
- Limitations derive from finite FPGA resources.
- Time granularity: 3.125 ns.
- Matching window common for all detectors.
- Employed in 2014 and in the current data taking with 99.96% efficiency.
- Currently operating @NA62 experiment at CERN.

**PC-based L0TP**
- FPGA receives L0 data while CPU performs trigger selection.
- Non real-time processing. 1 ms constant latency assured.
- Trigger matching algorithms software programmed.
- Large memory available.
- Full time granularity: 97.5 ps.
- Online selectable matching window for each detector.
- Designed for an upgrade of the experiment.
- Currently operating in parallel for testing.