The GigaTracker detector

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on behalf of the GTK group
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The NA62 experiment

Fixed target experiment: precision kaon physics @Cern SPS

Ultra rare K decays $K^+ \rightarrow \pi^+ \nu \bar{\nu}$

How rare is it? $1 \text{ in } 10^{10}-10^{11}$ particle decays

Aim to get $O(100)$ events in 2-3 years
The NA62 experiment

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GTK measures initial state kinematics and arrival time

It sees the whole beam!
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| **Beam rate** | 800 MHz - 1 GHz  
|              | 1.3 MHz/mm\(^2\) |
| **Radiation** | \( 10^{14} \) 1MeV eq n/cm\(^2\)/y |
| **Efficiency** | 99% |
| **Momentum resolution** | 0.2% |
| **Angular resolution** | 16 \( \mu \text{rad} \) |
| **Hit time resolution** | 200ps RMS |
| **Material Budget** | \( 3 \times 0.5\%X_0 \) |
| **Detector size** | 60mm \( \times \) 27mm |
Sensor-Chip Assembly

- Sensor [FBK,CIS]
  - Both p-in-n/n-in-p
  - Bias: 300 - 600 V
  - Thickness: 200 µm
  - MPV Charge per MIP: 2.4 fC

- Bump-bonding Sn-PB [IZM]

- 10 TDCPix chips/station: 130 nm CMOS [IBM] thinned at 100 µm

- Detector replaced every 100 days of beam (radiation)
The Front End Chip - TDCPix

-Design by Cern PH-EFE:
  -1800 pixels (40col × 45pix)
  -each pixel (300 × 300) µm²
  -separate analog-digital: no high freq clock to pixels
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  - amplifier (70mV/fC, 5ns peak. time)
  - discriminator
  - DAC threshold trim
  - configuration register
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  - time-to-digital converters (TDC)
  - data serializers
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**Power consumption:** ~3.5W, mostly EoC
Signals from 5 non adjacent pixels in a column are sent to a multiplexer (HitArbiter).

Each HitArbiter has a TDC pair measuring leading and trailing edges $\rightarrow$ 360 TDC pair/chip.

TDC have 100 ps bins.

Self triggered operation: rate 210 MHits/s.

Data sent out using four 3.2 Gb/s serializers.
Physics performance requires to **minimize the material budget**

Detector is in vacuum

Need to **dissipate ~35 W/station**

**Micro-channel cooling matches the constrains:**

- designed by Cern PH-DT group
- silicon-silicon assembly, (200 × 70) µm² channels
- low material budget: 130 µm of silicon (< 0.15% X₀)
The NA62 GigaTracker

Each GTK station is made of one hybrid silicon pixel detector (29.3 mm x 63.1 mm with 18000 pixels 300 μm x 300 μm) flip-chip bonded to 10 ASIC front-end chips TDCPix. Each station also includes a support structure, a cooling system and electrical and optical connections.

The GTK pixel detectors will be the first HEP detectors to be cooled with silicon microchannels. Liquid C₆F₁₄ will circulate at -20ºC in a 130 μm thick silicon plate with embedded microchannels (200 μm x 70 μm) to dissipate the heat produced by the electronics (power dissipation 40W).

Mechanical integration

- Detector glued on 130 μm Silicon Cooling Plate
- Cooling Plate is clamped onto PCB (isostatic)
- PCB is glued into frame and flange
- Flange closes the vacuum vessel
- Detector replaced every 100 days
Mechanical integration

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The NA62 GigaTracker

14th VCI

12/20
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The NA62 GigaTracker
14th VCI
12/20

Courtesy: J. Degrange
Electrical integration

- TDCPix wired bonded to PCB: dense wire-bonding scheme (73 \( \mu \text{m} \) pitch on chip)
- PCB routes power, clock, control and signal lines to/from the off-detector electronics
- Complex PCB:
  - 14 layers
  - 40 differential 3.2 Gb/s signals over 30 cm
Data acquisition - GTK-RO

- TDCPix sends out every hit: trigger matching needed
- GTK-RO built using FPGA (Altera Stratix GX110)
- Each GTK-RO made of two decked cards: daughter card handles interface with TTC
- Each TDCPix is connected to one DAQ board (GTK-RO) through 4 optical links (one per TDCPix 3.2 Gb/s serializer) + 1 configuration link. Transmission is data driven
GTK-RO board must

- buffer data, waiting for level-0 trigger decision (max level-0 trigger latency is 1 ms)
- retrieve data in a 75 ns time window upon each trigger request, and send them to the subdetector PC using UDP

Courtesy A. Cotta Ramusino
GTK-RO board must
- buffer data, waiting for level-0 trigger decision (max level-0 trigger latency is 1 ms)
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Assemble data from several GTK-ROs and send it to the online farm.

Plain linux distribution as O.S. with “zero copy” module of PF_RING to reduce memory to memory copy.

Multiple threads to handle the amount of data (worst case ~82 MB/s from each chip+protocol overhead).

Changes in 2016

Spikes in instantaneous beam intensity → use 2 PCs/station

Possibility to become L1-detector: GTK data not used for first sw trigger → readout GTK only in response to L1 triggers.
Results

- All stations + infrastructure installed and commissioned in 2015
- GTK cooled at 0 °C (2 g/s of C$_6$F$_{14}$ at 3 bar), thresholds set to 0.7 fC, bias voltage ~300V
- time resolution ≈ 215 ps @ 300V
Thank you for your attention
SPARES
NA62 signal and background

- **Signal:** \( m_{\text{miss}}^2 = (P_K - P_\pi)^2 \)

- **Background:**
  a) \( K^+ \) decay modes
  b) accidental single track matched with \( K \)-like one
Trigger and Data Acquisition (TDAQ)

**L0**: hw synchronous level. 10 MHz to 1 MHz. Max latency 1 ms

**L1**: sw level. “Single detector”. 1 MHz to 100 kHz. Max latency $O(1s)$

**L2**: sw level. “Complete information”. 100 kHz to 10 kHz. Max latency $O(30s)$
Time walk correction takes advantage of the relation between time walk and time-over-threshold.

Essential to meet the hit time resolution requirement.
Microfabrication of the cooling plates

- Plasma etching of channels & manifolds
- Bonding of Si cover
- Plasma etching of fluidic inlets
- Wet etching of acceptance
- Metallization around Inlets

Design by CERN PH-DT
Fabricated by CEA-Leti on 8” wafers