



# The tagging detector of the CP-violation experiment NA48 at CERN

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## Abstract

The CP-violation experiment NA48 at CERN aims at measuring direct CP-violation in the decays of neutral kaons into  $\pi^+\pi^-$  and  $\pi^0\pi^0$ . The experiment uses simultaneous, almost collinear beams of neutral  $K_L^0$  and  $K_S^0$  mesons, which are produced on two different targets.  $K_S^0$  events are “tagged” by measuring the times of the protons that fly towards the  $K_S^0$  production target. In order to sustain the high rate of  $10^7$  protons/s in this beam without suffering from too many pile-up events, the detector consists of 24 separate scintillators (12 horizontal and 12 vertical), each of which sees only a small fraction of the beam. Their signals are digitized by specially developed 1 GHz FADCs. The exact time of a pulse is established offline by a fit procedure. The detector and its electronics have been successfully used during test beams in 1994–1996 and during the first physics run of NA48 in 1997. The inefficiency of the detector has been measured to  $2 \times 10^{-4}$ . Sources of background have been identified to allow for off-line correction. The mechanical setup of the detector, the 1 GHz FADC and results from the test and data runs are presented. © 1998 Elsevier Science B.V. All rights reserved.

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## 1. Introduction

The NA48 experiment at the Super-Proton-Synchrotron accelerator of CERN (Geneva, Switzer-

land) studies direct CP-violation in the neutral kaon system by measuring the double ratio

$$R = \frac{|\eta_{00}|^2}{|\eta_{+-}|^2} = \frac{\Gamma(K_L \rightarrow \pi^0\pi^0)/\Gamma(K_S \rightarrow \pi^0\pi^0)}{\Gamma(K_L \rightarrow \pi^+\pi^-)/\Gamma(K_S \rightarrow \pi^+\pi^-)}$$

$$= 1 - 6 \operatorname{Re}\left(\frac{\varepsilon'}{\varepsilon}\right).$$

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Data taking for the  $\varepsilon'/\varepsilon$  measurement started in 1997 and will take a few more years to arrive at the projected error of  $2 \times 10^{-4}$ .

Kaons are produced by 450 GeV protons on two beryllium targets. In this process,  $K_L$  and  $K_S$  are always produced in equal amounts. To separate their contributions, the following method is applied.

A high-intensity proton beam of about  $10^{12}/s$  hits a first target (the “ $K_L$ ” target). The produced beam of neutral secondary particles passes through a long beampipe of about 120 m where all  $K_S$  decay. The part of the original proton beam that has not interacted in the  $K_L$  target is attenuated to an intensity of about  $10^7/s$  by a bending crystal and propagated parallel to the neutral beam until it hits a second target (the “ $K_S$ ” target) where again both kinds of neutral kaons are produced. The decay volume observed by the NA48 main detector (calorimeters, hodoscopes, driftchambers) is located right after the second target. Events are accepted if they decay within a few times the decay length of  $K_S$  mesons (about 5.4 m at an energy of 100 GeV). So nearly all the  $K_S$  produced at the second target will decay in this region while most of the  $K_L$  mesons produced here will pass on towards the beam dump without producing a signal (their decay length at this energy is about 3.1 km). The fact that only a tiny fraction of particles from the  $K_L$  beam decay in the fiducial volume, and the small branching ratio of CP-violating  $K_L \rightarrow \pi\pi$  decays are the reasons for which the proton beam at the  $K_L$  target has to be much more intense than the beam directed at the  $K_S$  target.

$K_S$  events are tagged by detecting the protons in the beam directed at the  $K_S$  target and considering the time of flight between the tagger and the main detector (hodoscope for charged events and liquid-krypton calorimeter for neutral events). If the time of an event recorded by the main detector is matched by the time of a proton seen in the tagger, the event is identified as a  $K_S$  decay. To guarantee the correct identification of events in spite of the long flight path (216 m between tagger and hodoscope, corresponding to about 720 ns) all detectors of the experiment use one synchronized, highly stable global clock [1].

## 2. The tagging detector

To avoid pile-up due to the high rate of over  $10^7$  protons/s in the  $K_S$  beam, an array of scintillation counters is used rather than a single scintillator. The tagging detector consists of a horizontal and a vertical “ladder” of thin scintillation counters, each of which is equipped with a light guide and a photomultiplier (Fig. 1). The signals of each photomultiplier are digitized by one Flash ADC module (see below). Normally, a proton gives rise to one signal in the horizontal and one signal in the vertical ladder. In this way the efficiency of the detector is maximized and the number of  $K_S$  decays wrongly identified as  $K_L$  decays is kept at a minimum.

Each scintillator sees only a narrow slice of the proton beam (Fig. 2) so that it has to cope with a rate of only 1–2 MHz. Neighboring scintillators overlap slightly to avoid inefficiencies. To match the intensity distribution in the proton beam, the innermost scintillators are very narrow (0.2 mm perpendicular to the beam) while the outer ones are somewhat broader (3 mm).

The scintillators are mounted on a carbon fiber structure produced by Stesalit company. The tagger structure was machined with an accuracy of  $\pm 5 \mu\text{m}$ . The tagging detector can be moved along three axes by a special high-precision system of motors to insure correct alignment with the proton beam.

## 3. The 1 GHz Flash-ADC

An 8-bit 1 GHz Flash-ADC module was developed for the tagging system to digitize photomultiplier pulses and to recognize superimposed double pulses of protons crossing the tagging detector [2]. The module contains two independent channels with up to 500 Megasamples per second implemented in commercial 8-bit/500 MHz hybrid FADC chips, each working with two internal 250 MHz data streams. They can be interleaved to obtain one channel with an effective sampling rate of up to 1 Gigasample per second (1 GHz; Fig. 3).

An external 1 GHz clock is divided by two and then used as the sampling frequency for each

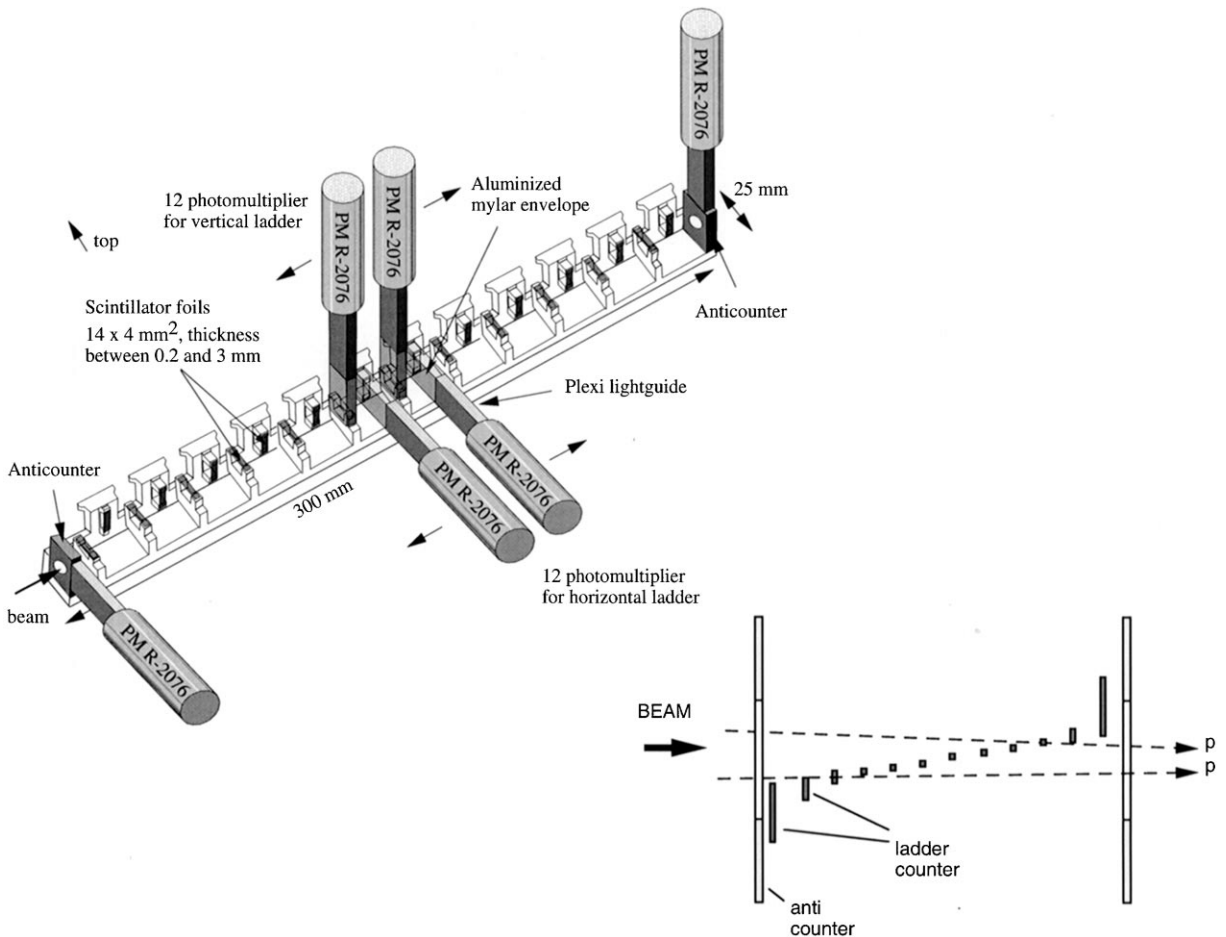


Fig. 1. The tagging detector.

channel. In NA48, the frequency actually delivered by the central clock is 960 MHz. For the sake of simplicity frequencies below are quoted for a 1 GHz clock input [1].

The external RESET signal is synchronised to the 1 GHz clock to give a precise starting point for the time information. During an external reset signal the synchronisation logic stops the 500 MHz clock. Then a few 250 MHz clock pulses are sent to the FADC chips to advance the internal states of both ADC chips to a predefined status and consequently to lock all four data streams to each other according to the selected sampling mode (interleaved or parallel). In addition, the reset signal is

distributed to all ringbuffer chips to lock all data bytes to each other in the correct time order.

To synchronise more FADC modules to each other, a common reset signal is used that is synchronised to the common clock.

The NA48 experiment requires that all data from the last 200  $\mu$ s have to be available on request. The data extraction must not generate any deadtime and must not destroy any information in order to allow a subsequent request to retrieve the same data samples again. Data should be available with or without zero-suppression.

A continuous sampling clock and a ring buffer memory running with interlaced write and read

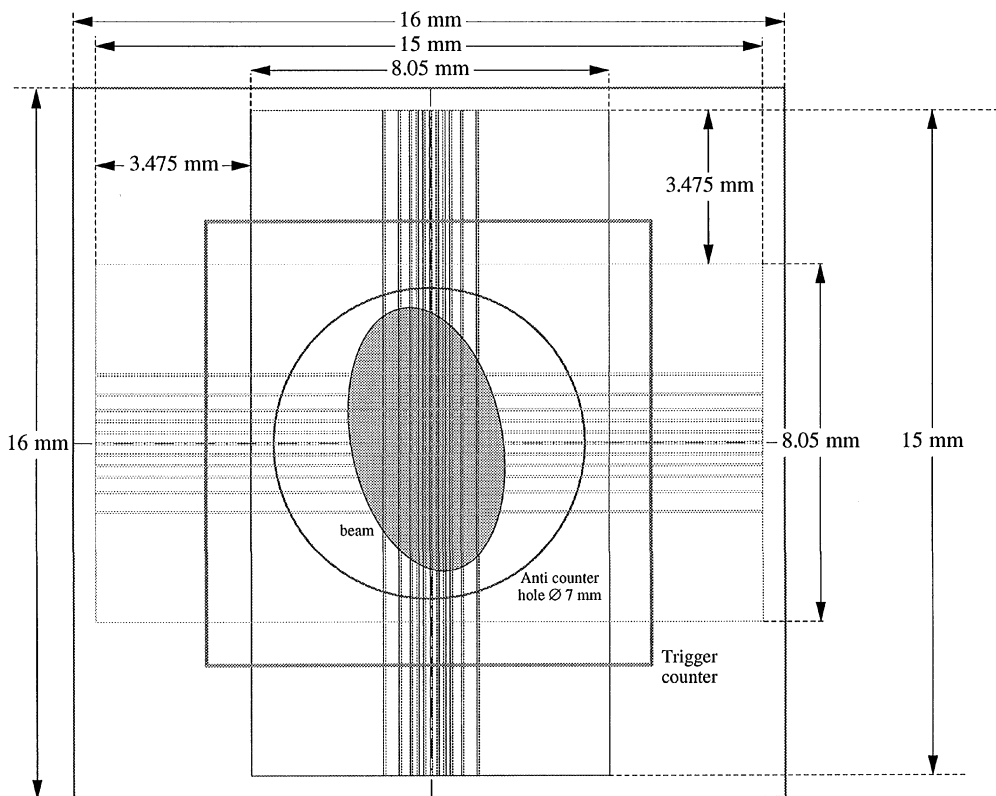


Fig. 2. The beam profile and the projections of the horizontal and vertical scintillators.

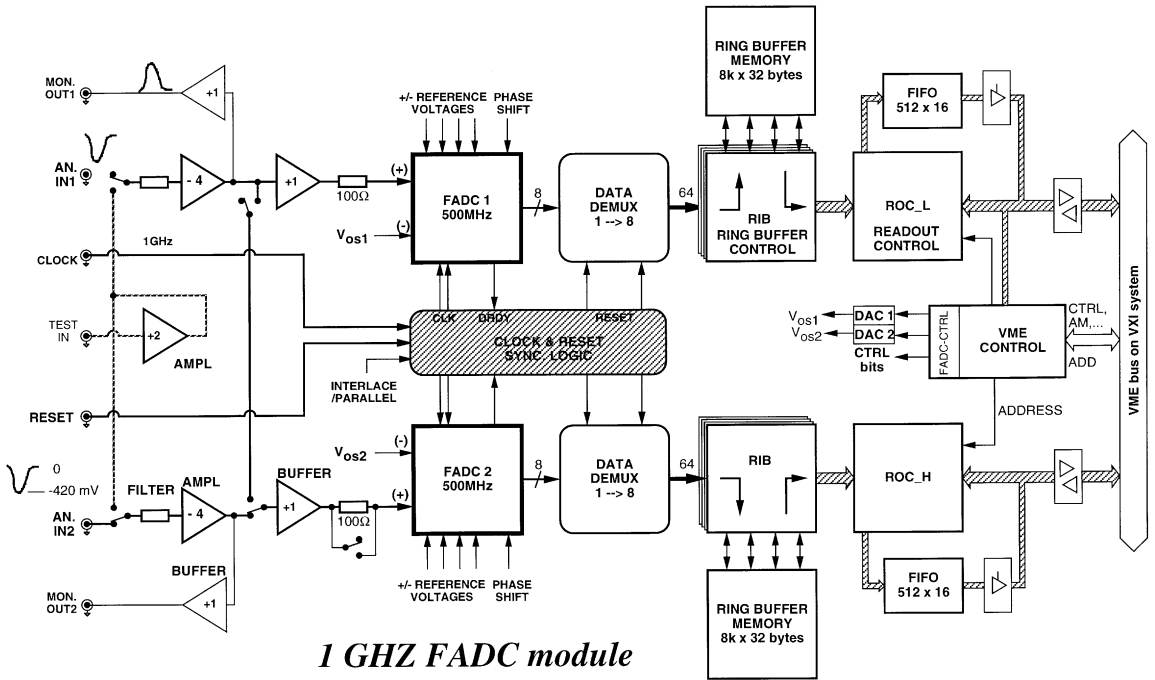
cycles fulfil all the requirements mentioned above. Each data sample enters the next free location of the memory. When the memory is full the next point will be stored at location one again and will overwrite the old content. The size of the memory has been selected to contain data from the last 524  $\mu$ s. To reduce the frequency of the write cycles, the 500 MHz data stream of each FADC chip is split into eight output streams of 62.5 MHz ECL signals. Then all data bytes are converted to TTL-level and transferred to the ringbuffer control chips (RIB) on daughter boards. An accompanying logic provides one clock signal for each pair of data bytes.

A ringbuffer control chip (RIB, Fig. 4) receives a pair of 62.5 MHz data streams and distributes each stream into four memory chips. Therefore, the word length of the ringbuffer is 32 bytes for each FADC chip. Each address of the ringbuffer is equivalent to a 64 ns time interval. The

position within the word defines the time for a sample in 2 ns units.

An external VME-master loads the desired time interval and control bits for the data extraction, such as the threshold for zero-suppression. Then it sends the start address into the ringbuffer address counters of both readout controller chips (= ROC). Each ROC transfers the address to four ringbuffer control chips (RIB). Between two successive write cycles the RIB-logic takes the address, inserts a read cycle and moves the contents of all memory chips into registers.

Each RIB chip contains a small counter to know which data point to put onto the output bus going to the readout controllers (ROC, Fig. 5). By means of these counters the data points are reordered in time. The ROC chip now sends data strobe pulses until all 32 bytes from all memory chips are transferred (20 MB/s). Then it sends the next address to



**1 GHz FADC module**

Fig. 3. Layout of the 1 GHz Flash ADC.

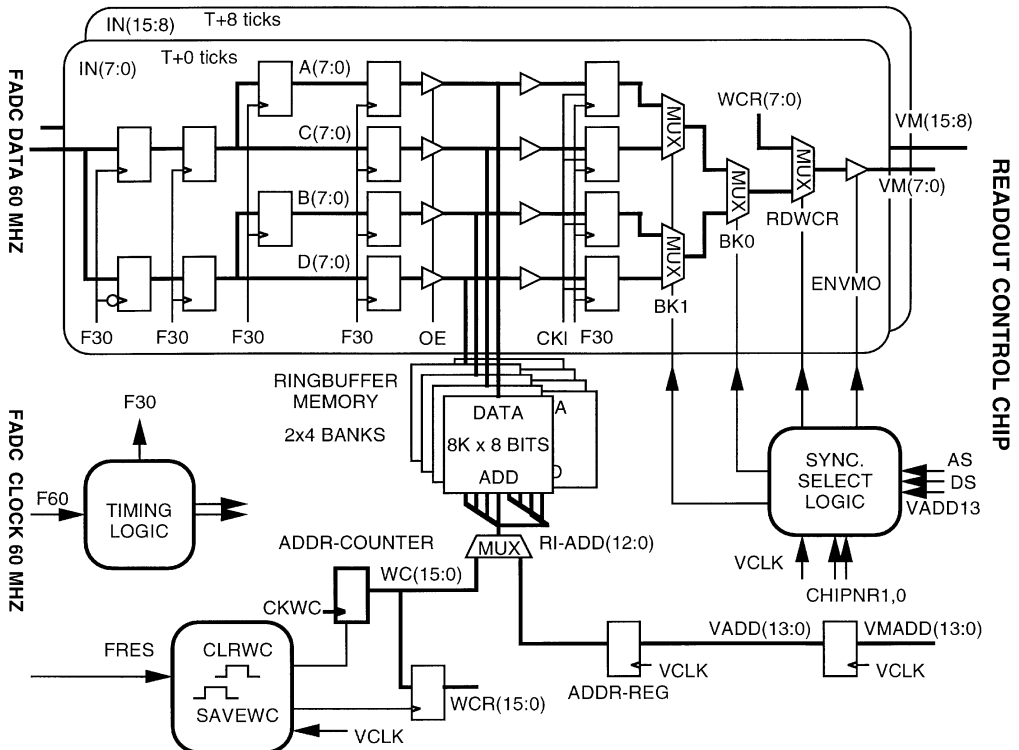


Fig. 4. The ringbuffer control chip and memory. One FADC chip sends data to four ringbuffer control chips with 32 memories in total.

Table 1  
Technical data of the FADC modules

Signal rise time	3–5 ns
Signal width	10–15 ns
Sampling rate (two – channel mode)	max. 500 Megasamples per second
Sampling rate (interleaved mode)	max. 1 Gigasample per second
External clock – frequency range	800 MHz–1 GHz
Length of external reset (ECL)	200 ns
Amplitude resolution	8 bits
Analog bandwidth	180 MHz
Input voltage range (unipolar)	0–0.42 V (max)
Input voltage range (bipolar)	(–0.21)–(+0.21) V
Input impedance (each channel)	50 $\Omega$
Ring buffer memory depth	512 k byte
Event recording time at 1 GSPS	524 $\mu$ s
Intrinsic time resolution	30 ps (rms)
Module standard	VXI D-size
Interfaces	VME, VXI local bus

the RIB controllers and so on until all points from the selected time interval are read.

The ROC checks the incoming data and removes all points below the threshold. Two points adjacent to valid pulses are taken to reconstruct pulses correctly. Then it adds the fine time bits to each data byte, composes all format words and finally writes the complete information into 16-bit FIFO memories.

Data from a typical time window of about 100 ns are extracted in less than 3  $\mu$ s. The VME slave interface has been designed to read data from the FIFO memories with a rate of up to 32 MB/s. To accelerate the data readout, a special subaddress allows to simultaneously set up all cards inside one crate (broadcast write) within 2 VME write cycles. The same subaddress is used to read the FIFO memories from all cards inside one crate by one block transfer. Modules without relevant data can be excluded automatically from the readout procedure. Normally the programmed length of the block transfer exceeds the data length. An EMPTY signal of the last module goes to the interrupt input of the reading VME-master and stops the block transfer immediately when the last module in the crate becomes empty. A maximum differential non-linearity of less than 0.5 LSB (least significant bits) was measured and no missing codes were found.

The 30 FADC modules (Table 1) used to read out all the photomultipliers are housed in three VXI-crates (Fig. 6). These crates are controlled via a VME-crate. The data are read out by fast RISC processors (one per crate) and transferred to a special interface (VFIFO), which sends them via a long optical link to the central data recording unit.

## 4. Data analysis and results

### 4.1. Scintillator pulses

Fig. 7 shows a typical pulse from a proton passing the tagging detector, digitized by one of the 1 GHz FADCs. During normal data taking a zero-suppression logic removes all data below an adjustable threshold unless they are within 2 timeslices of an above-threshold sample. (This allows to efficiently reduce the data volume and still measure the baseline of the FADCs.) For detailed detector studies (e.g., investigation of electronic noise) the zero-suppression mechanism can be turned off as shown here. To determine the time of a proton passing the tagging detector, all pulses recorded for the corresponding time interval are fitted during offline analysis by a convolution of an exponential and a Gaussian [3]. The proton time is obtained by

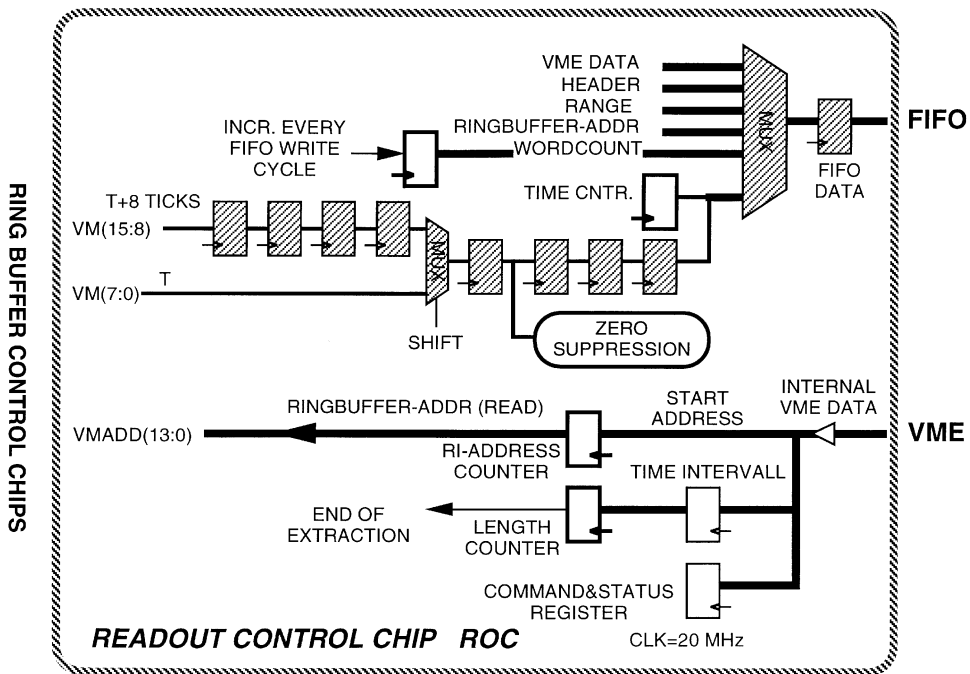


Fig. 5. The readout control chip.

averaging over times measured by tagger scintillators within a narrow coincidence interval (in this case the scintillators are assumed to have been hit by the same proton).

#### 4.2. Time resolution and detector efficiency

In case of inefficiencies  $K_S$  decays will be misidentified as  $K_L$  decays while accidental hits in the tagging detector will lead to a misidentification of  $K_L$  decays as  $K_S$  decays. The inefficiency is reduced by using the logical “OR” of the horizontal and vertical ladders. “Accidental” hits are mostly due to the  $K_S$ -proton beam itself. So no protons must be lost, and at the same time the time window for a coincidence between the NA48 main detector and the tagger must be kept as small as possible. This requires a very good time resolution of the tagging system. Fig. 8 shows the difference in the time measured for  $K_S$  decays into two charged pions and the time given by the tagger for the corresponding proton. As seen from the Gaussian fit, the time resolution is about 200 ps. When selecting a coin-

cidence window of  $\pm 2$  ns, the inefficiency of the tagging system is about  $2 \times 10^{-4}$ .

#### 4.3. Double-pulse separation

Unresolved double pulses in the tagging detector may result in wrong timing of protons and consequently in mistagging of kaon decays. So along with efficiency and overall time resolution, the double-pulse separating power is an important parameter for the performance of the tagging detector. Fig. 9 illustrates the double-pulse resolving power in a single counter of the tagging detector.

The protons crossing the tagging detector are random in time as long as they do not generate a  $K_S$  which causes a trigger, so the time difference between any proton and the next one should follow an exponential function. The solid line shows the resolving power of a simple peak-finding algorithm. The 5 ns structure visible in the plot is due to the accelerator’s RF-frequency. Significantly better double-pulse separation is achieved by trying

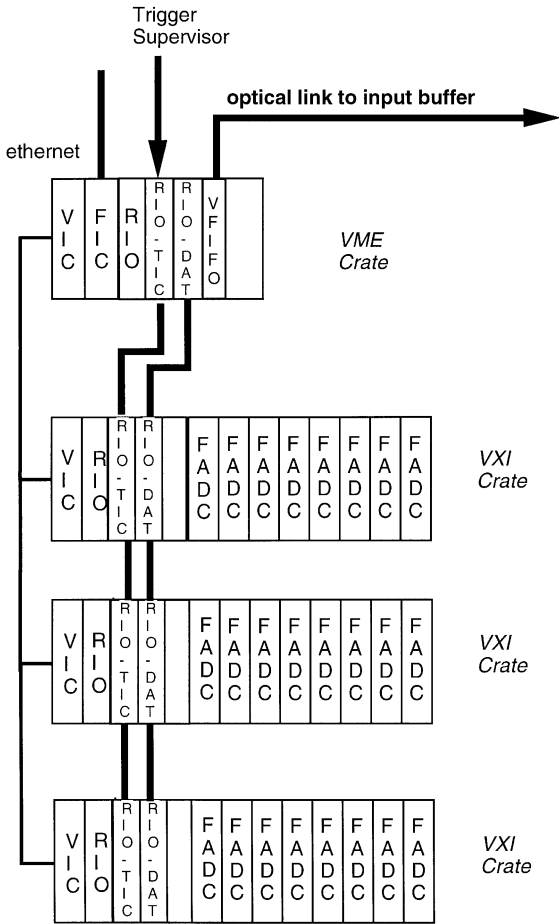


Fig. 6. Setup of the tagger readout electronics.

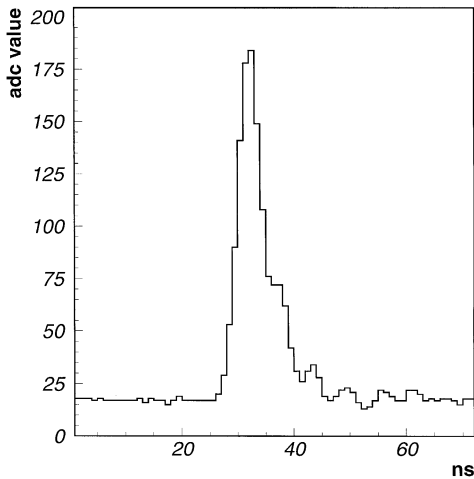


Fig. 7. Typical proton pulse seen by the FADC.

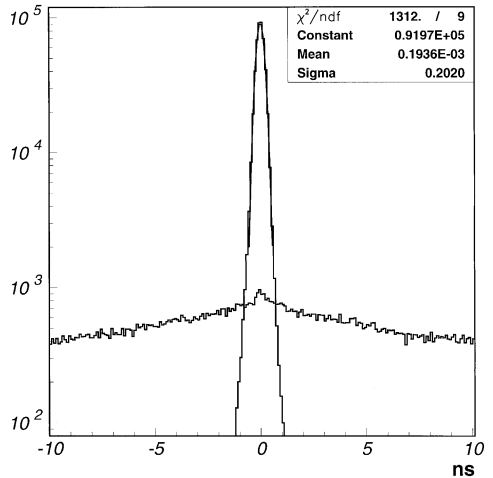


Fig. 8. Time resolution of the NA48 tagging system for charged particles. The peak is from identified  $K_S$  events, the flat distribution is background from  $K_L$  events.

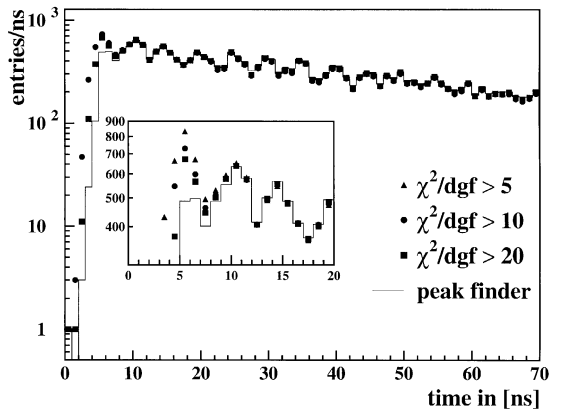


Fig. 9. Double-pulse separation.

to fit an event with two pulses when the first fit yields a value of  $\chi^2/n_f$  (chi-squared over number of degrees of freedom) above a certain limit (triangles, dots and squares in the plot). The double-pulse fit is retained when  $\chi^2/n_f$  is improved by more than 2. The double-pulse separation depends on the limiting value in  $\chi^2/n_f$ : setting this value too high one may miss a double pulse, taking it too low may create spurious double pulses. The optimum value was found to be  $\chi^2/n_f = 10$ .

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## **References**

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