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Review of results for the NA62 gigatracker read-out prototype

E. Martin,[a,1] **G. Aglieri Rinella,**[b] **V. Carassiti,**[d] **A. Ceccucci,**[b] **E. Cortina Gil,**[a] **A. Cotta Ramusino,**[d] **G. Dellacasa,**[c] **M. Fiorini,**[a] **S. Garbolino,**[c] **P. Jarron,**[c] **J. Kaplon,**[b] **A. Kluge,**[b] **F. Marchetto,**[c] **A. Mapelli,**[b] **G. Mazza,**[c] **M. Morel,**[b] **M. Noy,**[b] **G. Nuessle,**[a] **P. Petagna,**[b] **F. Petrucci,**[d] **L. Perktold,**[b] **P. Riedler,**[b] **A. Rivetti,**[c] **M. Statera**[d] **and B. Velghe**[a]

[a] *Université Catholique de Louvain,*
Chemin du Cyclotron 2 1348 Louvain-la-Neuve, Belgium
[b] *CERN,*
CH-1211 Geneva 23, Switzerland
[c] *INFN Sezione di Torino,*
Torino, Italy
[d] *INFN Sezione di Ferrara,*
Ferrara, Italy

E-mail: elena.martin.albarran@gmail.com

ABSTRACT: The Gigatracker (GTK) is a hybrid silicon pixel detector developed for NA62, an experiment studying ultra-rare kaon decays at the CERN SPS. The main characteristics are a time-tagging resoluion of 150ps, with low material budget per station (0.5% X_0) and a fluence comparable to the one expected for the inner trackers of LHC detectors in 10 years of operation. To compensate the time-walk, two read-out architectures have been designed and produced. The first architecture is based on a Constant Fraction Discriminator (CFD) followed by an on-pixel Time-to-Digital-Converter (TDC). The second architecture is based on a on-pixel group shared TDC. The GTK system developments are described: the integration steps (assembly and cooling) and the results obtained from the prototypes fabricated for the two read-out architectures.

KEYWORDS: VLSI circuits; Front-end electronics for detector readout

[1] Corresponding author, now at the Universitat Autonoma of Barcelona, UAB.

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1 Introduction to NA62

The very rare kaon decay $K^+ = \pi^+ \nu\overline{\nu}$ is a process which can help to understand the flavor structure of possible physics beyond the Standard Model. The fixed target experiment NA62 [1], located at CERN, aims to measure ∼80–100 events of this decay over 2 year of data taking. The Standard Model expectation for the branching ratio of this decay is $\mathrm{Br}(K^+ \to \pi^+ \nu\overline{\nu}) = (7.81 + 0.80 \pm 0.29) \times 10^{-11}$ [2]. Such a measurement requires rejection factors of the main kaon decays of the order of 10^{-10}.

A high intensity kaon beam has been developed in order to provide the $\sim 10^{13}$ kaon decays needed. The kaon beam will be generated by impinging 400 GeV/c protons from CERN SPS on a beryllium target, where 75 ±0.8 GeV/c positive charged particles will be selected selected at the entrance to the decay line. Only 6% of the particles selected will be kaons. The beam generated will have an expected instantaneous intensity of ∼ 800 MHz. This high intensity imposes constraints on the timing of the detectors, especially in the detectors located upstream that should have time resolutions better than 200 ps. Kaon decays will happen in a vacuum tube instrumented with various detectors. A full description of the NA62 apparatus as well as the beam can be found in [3].

1.1 General description of the GigaTracker detector

The NA62 experiment consists of many detectors, from a CEDAR counter to identify the K^+ component of the incoming beam, to the charged-particle hodoscope (CHOD), used to cover the acceptance and located between the RICH and the LKr calorimeter. After the CEDAR counter is found the GigaTracker, the GTK has been designed to measure the momentum, angle and traversal time of the incident particles entering the decay line from the target, by using three stations situated early in the experiment decay line, see figure 1.

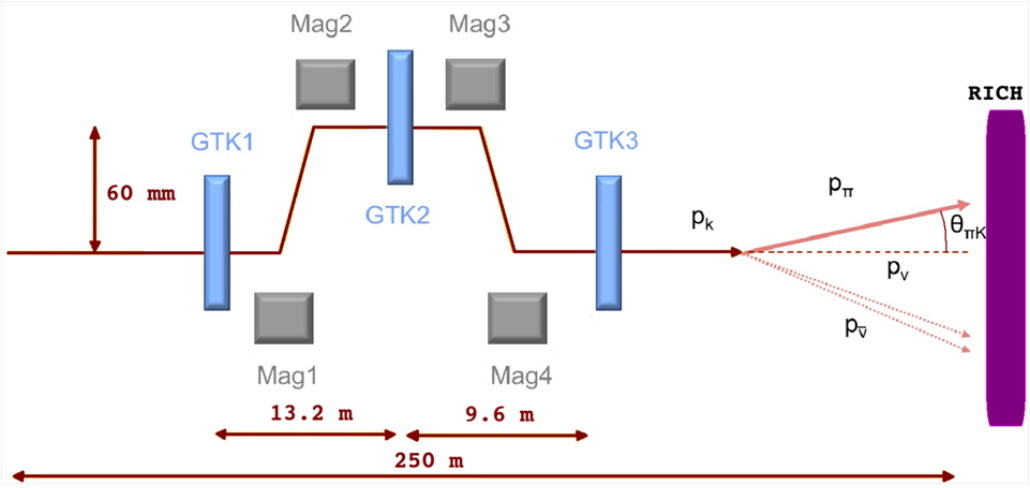

Figure 1. Schematic of the GigaTracker showing the distribution of the different elements: stations and magnets. The last part shows the RICH used.

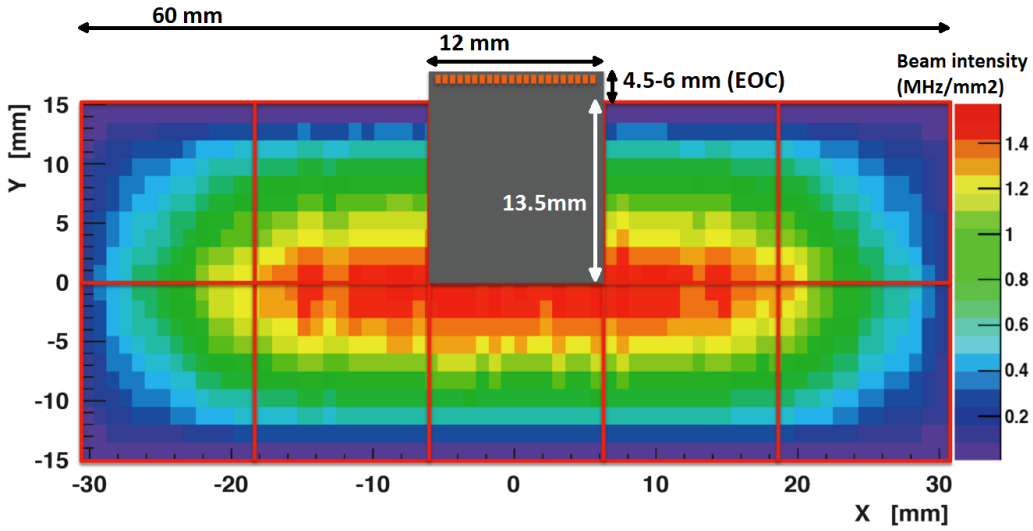

Figure 2. Expected beam rate intensity distribution at the stations, with the sizes of the detectors. The grey part of the figure corresponds to the read-out circuitry that will not be exposed to the center beam.

The specifications of this detector are defined by the large background rejection level to be achieved [4]. The main characteristics are an incident beam rate which is expected to be $\sim$ 800 MHz, which equates to approximately 140 kHz per pixel in the centre (where the maximum intensity is found, as shown in figure 2). Each detector will have an area of $60\times27\text{mm}^2$ and consists of an array of 18000 pixels, with a 300 $\times$ 300 mm^2 area per pixel. This detector area will be read-out by 2 rows of 5 readout chips and the read-out circuitry will process input charge with a dynamic range from 5000 e^- to 60000 e^-. Time stamping resolution is required to be 200 ps (RMS) for each station, and this information will be correlated with the RICH to reduce combinatorics.

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2 GigaTracker read-out ASIC demonstrator

As has been already mentioned, the GTK requirements are very challenging in terms of timing resolution, particle rate and radiation exposure, but also for the low material budget. A more detailed analysis of these requirements includes the following aspects: high data transmission rate and high power consumption. The high data transmission rate can be approximated with the following calculation. If every hit is encoded into a 40-bit word the data throughput will reach the considerable value of 6.3 Gb/s per chip, which means 7.5 Gb/s considering a serial transmission with a 8b/10b encoding. At this rate the use of high speed differential signal is mandatory and a triggerless readout will be adopted. Also power consumption is an issue while the cooling system puts a limit on the overall dissipation in the GTK station of 2W/cm^2. In addition the chips have to operate in a strong radiation environment, with an expected total dose of 10^5 Gy in one year.

The GTK pixel readout chip will be implemented using the CMOS 130 nm technology. Several studies on this technology showed that it should be sufficiently radiation hard for the expected total dose from kaons and pions with a background of neutrons. However, the dose is not uniform in the three stations or in the centre or periphery of each chip. This will cause a different response from pixels located in different positions that can be adjusted by trimming the discriminator threshold on each pixel. The required timing precision and high hit rate impose the use of a fast transimpedance amplifier with a very short peaking time, limiting the time walk of the comparator. The lower limit for the value of the peaking time is determined by the achievable charge collection time from the Silicon detector. The charge collection time is defined by the thickness of the detector, in this case the detector is thinned down to 200 μm. This thickness is the one limiting the signal speed in the sensor, and is defining the optimum value of the peaking time for the shaper.

2.1 General description: assembly, cooling and read-out

The three aspects that define the detector system are based on the assembly, the cooling and the electronics. The detector consists of a hybrid pixel system. The sensor is bump-bounded to the read-out circuit, where each one of the detectors is read-out by 10 chips. One of the main concerns in this experiment is the material budget, and a 200 μm thick sensor with a 100 μm ASIC thickness will be used to achive a total material budget $<0.5\%$ X_0. The detector has to operate in over-depletion, in order to achieve the time resolution, with a value of 300V over-bias. This voltage applied will enable fast charge collection. For the cooling, the GTK stations will be installed in vacuum, with high and non-uniform radiation levels and an expectence expected fluence is of $\sim$2 $\times$ 10^{14} (1 MeV n_{eq}/cm^2) during one year of operation in the sensor center. Two cooling options are under study: gas cooling (the cooling is done via flow of cold gaseous nitrogen in a thin cylindrical kapton windows in an aluminum vessel frame) and micro-channel cooling [5] (based on 2 bonded Si wafers where micro-channels, as well as through holes for fluidic inlets/outlets, are etched in one wafer and the second wafer is bonded as a cover to close the channels). These characteristics are defining the overall mechanical design, considering each module will have to be replaced and removed with minimal intervention [6].

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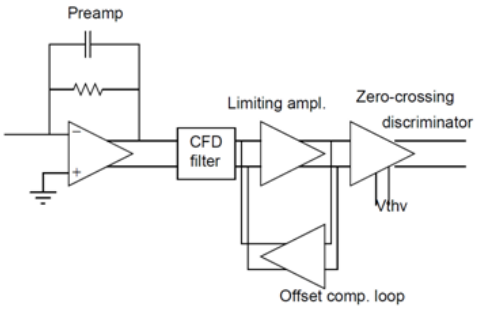

Figure 3. Schematic of the pixel architecture used in the in-pixel TDC

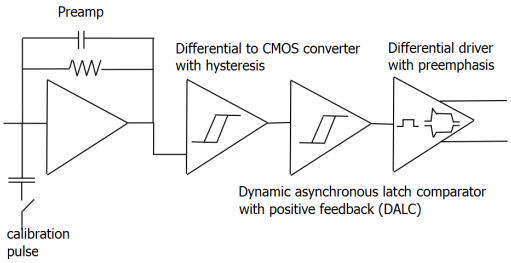

Figure 4. Schematic of the pixel architecture used in the End of Column TDC

2.2 Read-out electronics

The design of the read-out is constrained by the effect of time walk, combined with the time resolution and dynamic range. The time walk effect has to be compensated, and two techniques have been proposed. These options are the measurement of time over threshold (TOT) and the use of a CFD. The TOT technique uses a preamplifier, where the output signal width is proportional to the input signal amplitude. The time walk correction is based on an algorithm derived from the correlation between the pulse width and the resulting time walk that can be measured when injecting signals with known amplitude. The CFD filter uses the inversion of one portion of the input signal, while the signal is delayed by a fixed time. The signals are combined with a zero crossing point that is independent of the input charge. For the GTK readout chips both techniques have shown promising results and these will be presented in the section 3 and section 4.

The first option evaluated, the so-called CFD [7–9], see figure 3, is based on a complex per pixel architecture, that includes an CFD filter and a TDC based on a fine time measurement obtained by a time to amplitude converter (TAC). This approach intends to maximize the signal processing on the pixel cell. The main disadvantages of this approach are related to the need of a strong and low noise clock distribution and the complexity of a radiation-tolerant column logic. The main advantage is that there is no need of propagating the comparator signal outside the pixel.

The second option, the so called End of column TDC [10–12], see figure 4, is based on a ToT architecture where the Delay Locked Loop (DLL) and the high precision TDC is shared among groups of pixels. This option tries to minimize the on-pixel processing to minimize the noise. By doing that, the system has to propagate the comparator signal to the periphery of the chip using ultra-fast transmission lines.

3 Constant fraction discriminator architecture

The CFD architecture uses an on-pixel Wilkinson TDC. This architecture has been tested with a prototype chip that included 2 test pixels, a pixel matrix of 1×15 cells, another pixel matrix of 2×45 cells and the logic. It was designed for a dynamic range of 1-10fC, with an area for the CFD of $154\mu\text{m}\times74\mu\text{m}$. The electrical results obtained for a single pixel show a jitter at 1MIP of 90ps rms, as can be seen in figure 6 and a time walk of 92ps for 2.4fC electrical input charge [7].

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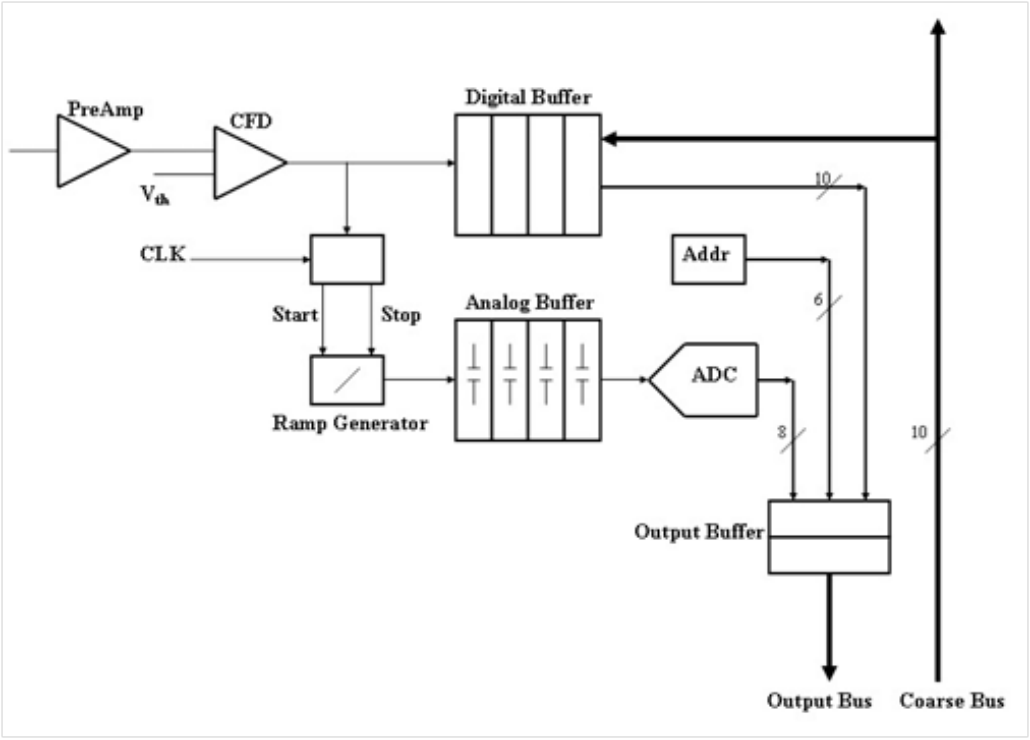

Figure 5. Block diagram of the CFD pixel cell with a 4-buffer scheme used for multi-event data handling.

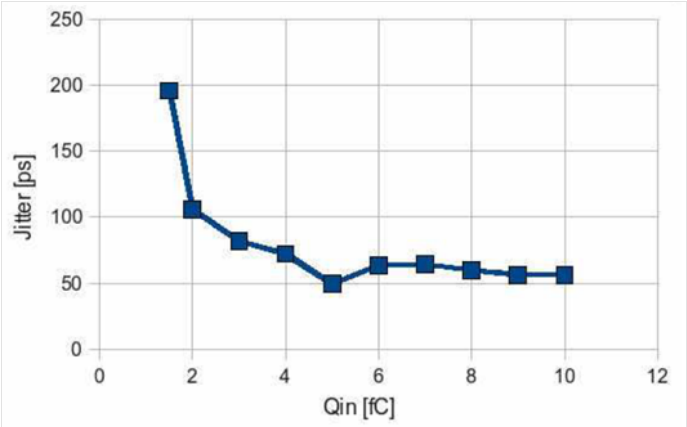

Figure 6. Typical jitter measured from a pixel in the CFD matrix showing a rms value of 75ps for 2.4fC.

This prototype has been re-designed to improve the performance of the CFD. This second design intends to improve the time precision by making the CFD more robust to shape variations. This architecture has not been fabricated yet, but simulations show improvements in terms of correcting time-walk and fluctuations induced by shape variations as can be seen in table 1.

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Table 1. Simulation results obtained with 200 input signals generated with Montecarlo for amplitude variations and shape variations coming from statistical fluctuations in the charge released along the sensor and to non-uniformity in the electrical field at the borders of it.

Process corner	RMS jitter$_{1MIP}$(ps)	Time resolutions(ps)
Typical mean	65	29
+3σ	79	25
-3σ	68	26

4 End of column architecture

The architecture of the second option is divided in two parts [11], the pixel matrix and the End of Column logic, see figure 7. This architecture was implemented and tested in a prototype with the following specifications. The pixel cell is formed by 7 functional blocks that consume a total of 120μA and the general architecture can be summarized as a transimpedance preamplifier using a feedback capacitor of 14fF and a feedback resistor of 200kΩ, a first differential post amplifier, a first stage of the discriminator, a second stage of the discriminator with hysteresis, a dynamic asynchronous latch comparator with transitional positive feedback, a differential transmission line current driver with pre-emphasis that needs 100μA and a coplanar transmission line. The transmission line receiver generates the pulses with edges of 50ps to drive the TDC inputs. The arrival time is measured using delay locked loop (DLL) based TDCs, where buffers connected in series are used as base elements, with a delay per cell of $\sim$97.65ps. Each TDC consists of two 32-bit hit registers that provide double time stamping. In addition at the time of the leading and trailing edge the coarse clock counter value is latched, increasing the dynamic range. The double time stamp with coarse counter and address information are stored in a line buffer, which is then serialized and sent off chip.The TDC performance also was evaluated by measuring the non-linearities, and the results showed a differential non-linearity (DNL$_{RMS}$) of 0.17 LSBs and an integral non-linearity (INL$_{RMS}$) of 0.27 LSBs, with an estimated RMS jitter better than 10ps.

This prototype has been tested electrically, with a infrared laser and in a beam test environment. The electrical test included the measurement of the time walk values [14], the study of the nonlinearities of the TDC and the variation of the gain for different injection times. The measurements of the time walk results have been obtained by performing electrical and laser charge injection. The electrical charge injection was done with no detector bump-bonded and results are presented in figure 8, they show a leading edge time jitter T_1 of 40ps rms at 2.4fC. The laser injection measurement with the detector bump-bonded and biased at 300V showed a jitter at T_1 of 70 ps RMS at 2.4pC with a good jitter performance over the full range of interest. The relation between pixel gain and injected charge time was studied, see figure 9, and a gain of 72mV/fC was measured, with a σ=1.5mV/fC. The noise was measured with no sensor to be 130e$^-$, and with sensor increased to 180e$^-$. These values are consistent with the ones expected for a detector capacitance of 250fF. The results obtained for the bump-bonded system with the pixel center illuminated have been compensated for time walk effects, resulting in a time resolution of $\sim$70 ps at 2.4fC for all the pixel chain. This results considers systematic compensation error and the statistical fluctuation due

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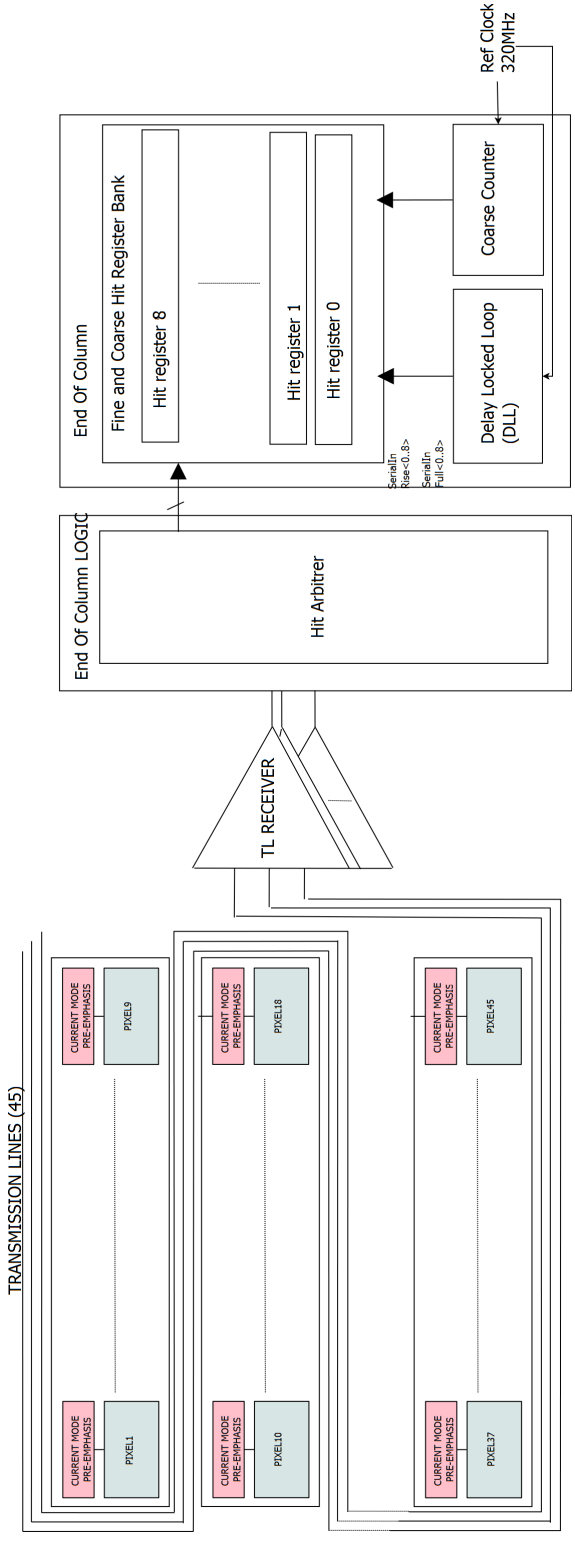

Figure 7. Block diagram of the general pixel matrix architecture, where the pixel area and the end of logic circuitry is clearly separated.

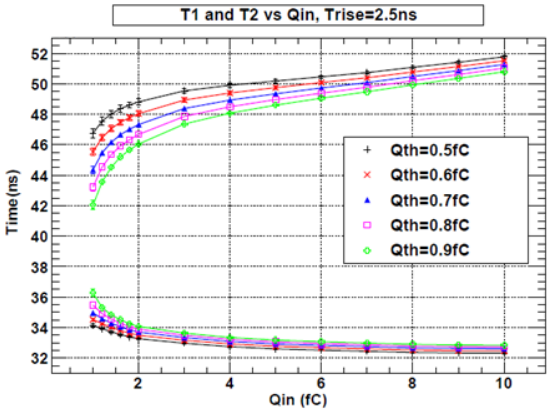

Figure 8. Leading (T1) and trailing edge (T2) time, for different threshold charges, measured at the discriminator output, with a rising time for the injected charge of 2.5ns. The peak-to-peak variation for T1 is 2.2 ns.

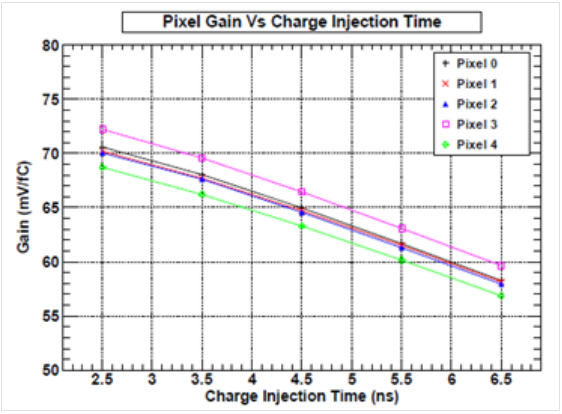

Figure 9. Measurement of the Gain vs Charge pulse duration for a injected charge of 2.4fC. These results show ballistic deficit from past peaking time.

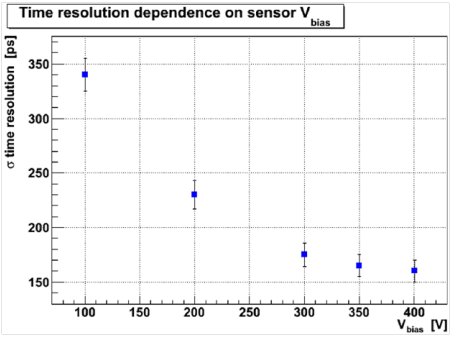

Figure 10. Measured time resolution for different detector bias. In this measurements the hole drift speed is not fully saturated and not all the assemblies could tolerate to work at 400V.

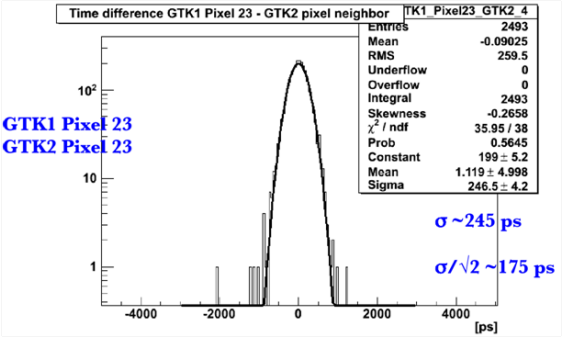

Figure 11. Measured time resolution with beam particles not considering hit clustering. This results correspond to the same position pixel located in 2 different assemblies.

to noise and jitter with a detector bias of 300V. Additional geometrical studies have been performed with an x and y axis scan using Landay weighting to emulate the charge specturm seen at the beam test, as will be shown in next results, giving a value of 70ps that agrees with previous results.

Two fast scintillators with 25 ps binning time were used to have a very precise time reference. The results obtained for the time resolution, show a large dependence on the bias of the detector, as can be seen in figure 10. The target time resolution of 200ps and the results obtained indicate that the system has to work with an applied voltage of 300V. The measurements obtained after applying compensation for time walk effects resulted in a time resolution of 175ps, see figure 11, which is a value below the original target. This value are significantly different to the expectations from laser setup, of 75ps, as the timining resolution is dominated by random fluctuations of the sensor current shape [15]. This shape is defined by the position of the track hit in the pixel and the charge straggling .

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5 Conclusions

The GTK read-out demonstrator is evaluating two different solutions. The first solution considers the use of a CFD and a complex pixel architecture, that is trying to maximize the pixel digital logic. This solution has been electrically tested for a single pixel, with no clock and based on these results, another prototype is being development with a target time resolution below 50ps. The second solution considers the use of the ToT per pixel, minimizing the digital logic per pixel and using transmision lines to send the data to the end of column logic. This solution has also been tested as a full system in a beam, and the first prototype measurements have shown time resolution in beam test consistently lower than 200ps. This solution has shown a more robust behaviour and improved real detector size circuit will be submitted for fabrication for the beginning of 2012.

References

[1] G. Anelli et al., *Proposal to measure the rare decay* $K^+ \to \pi^+ \nu\bar{\nu}$.

[2] J. Brod, M. Gorbahn and E. Stamou, *Two-Loop Electroweak Corrections for the* $K \to \pi\nu\bar{n}u$ *Decays*, *Phys. Rev.* **D 83** (2011) 034030.

[3] NA62 collaboration, E. Cortina et al., *NA62 Technical Design*, http://na62.web.cern.ch/na62/Documents/TechnicalDesign.html.

[4] M. Fiorini et al., *The P326 (NA48/3) Gigatracker: Requirements and design concept*, *Nucl. Instrum. Meth.* **A 572** (2007) 290.

[5] A. Mapelli et al., *Novel low material budget microfabricated cooling devices for particle detectors and front-end electronics*,*Nucl. Phys. B Proc. Suppl.* **215** (2011) 349.

[6] M. Morel et al., *The electro-mechanical integration of the NA62 GigaTracker time tagging pixel detector*, 2010 *JINST* **5** C12023.

[7] A. Rivetti et al., *Experimental Results from a Pixel Front-End for the NA62 Experiment with On Pixel Constant-Fraction-Discriminator and 100ps Time-to-Digital-Converter*, *IEEE Nucl. Sci. Symp. Conf. Rec.* (2010) 400.

[8] G. Mazza et al, *A Silicon Pixel Readout ASIC with 100ps Time Resolution for the NA62 Experiment*, 2011 *JINST* **6** C01087.

[9] G. Dellacasa et al., *A 130nm ASIC Prototype for the NA62 Gigatracker Readout*, *Nucl. Instrum. Meth.* **A 650** (2011) 115.

[10] P. Jarron et al., *Development of the ASICs for the NA62 pixel Gigatracker*, in *Topical Workshop on Electronics for Particle Physics*, Naxos, Greece, 15–19 Sept. 2008, pp.90-94, http://cdsweb.cern.ch/record/1158509/.

[11] E. Martin et al., *The 5ns peaking time transimpedance front end amplifier for the silicon pixel detector in the NA62 Gigatracker*, *IEEE Nucl. Sci. Symp. Conf. Rec.* (2009) 381.

[12] M. Fiorini et al., *Results from the NA62 Gigatracker prototype: a low-mass and sub-ns time resolution silicon pixel detector*, Presentation at the Technology and Instrumentation in Particle Physics, Chicago, Jun. 2011, http://indico.cern.ch/materialDisplay.py?contribId=55&sessionId=22&materialId=slides&confId=102998.

2012 JINST 7 C03030

[13] S. Garbolini et al., *Results from the NA62 Gigatracker prototype*, Presentation at the *10th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors*, July 6-8, 2011, Firenze Italy.

[14] M. Noy et al., *Characterisation Of The NA62 GigaTracker End Of Column Readout ASIC*, *Nucl. Phys. B Proc. Suppl.* **215** (2011) 198.

[15] G Aglieri Rinella et al., *The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatracker of the NA62 experiment*, Presentation at the TIPP 2011, 2nd Internatioal Conference on Technology and Instrumentation in Particle Physics, http://indico.cern.ch/contributionDisplay.py?contribId=369&sessionId=23&confId=102998.

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