READOUT ELECTRONICS OF THE NA62 GIGATRACKER SYSTEM

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A crucial detector of the NA62 experiment is the beam spectrometer named Gigatracker. It consists of three stations of hybrid silicon pixels sensors with 150 ps (rms) of time resolution and 100 μm (rms) of space resolution. In addition the system operates under a high radiation environment and a high density of particles (up to 1.5 MHz/mm^2 in the centre and 0.8 - 1 GHz in total). To meet these requirements the readout electronics must compensate the discriminators time-walk and the dead time should be below 1%. In order to evaluate the best solution, two readout chips have been developed. One is based on the constant-fraction discriminator technique and the other one is based on the use of a time-over-threshold circuit. The global architectures of both the front-end ASIC will be discussed.

1. The Gigatracker system

The NA62 experiment at CERN SPS aims to collect more than 80 events of the very rare decay of the charged K meson into a pion and neutrino-antineutrino pair, in order to obtain a direct measurement of the CKM matrix parameter Vtd[1]. A crucial detector of the NA62 experiment is the beam spectrometer named Gigatracker. It consists of three stations (Figure 1) of hybrid silicon pixels

sensors with an overall 150 ps (rms) time resolution and 100 μm (rms) space resolution. In addition the system will operate under a high radiation environment due to the high density of particles (up to 1.5 MHz/mm^2 in the centre corresponding to 0.8 - 1 GHz in total). In order to partly recover the radiations effects (10^5 Gy of total dose is expected in one year) the system will be cooled at 5^o C or less and it will be replaced after a runtime of 60 days under optimum beam conditions.

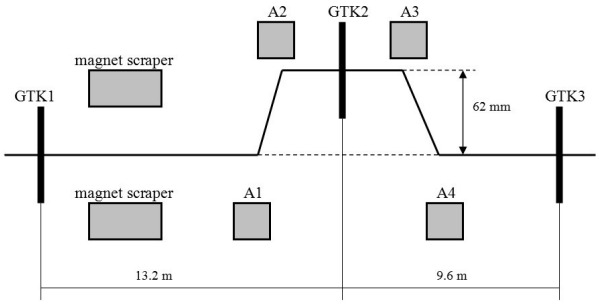

Figure 1. Gigatracker system

Each station consists of a 45x40 pixels matrix corresponding to a total area of 60 mm x 27 mm, which covers the asymmetric beam profile with no dead areas . Each pixel is 300 μm x 300 μm. The detector operates in vacuum and the total thickness is 300 μm (200 μm the sensor and 100 μm the readout chips) which is less than 0.5% of the radiation length per station [2].

The beam area is covered by a 2x5 matrix of readout ASICs bump bonded to a single detector (Figure 2). Each readout chip has a sensitive area of 12 mm x 13.5 mm. The particle rate, which is higher in the central part of the sensor, is estimated to be ~1.5 MHz/mm^2 maximum, which corresponds to 130 MHz per chip and 140 kHz per pixel.

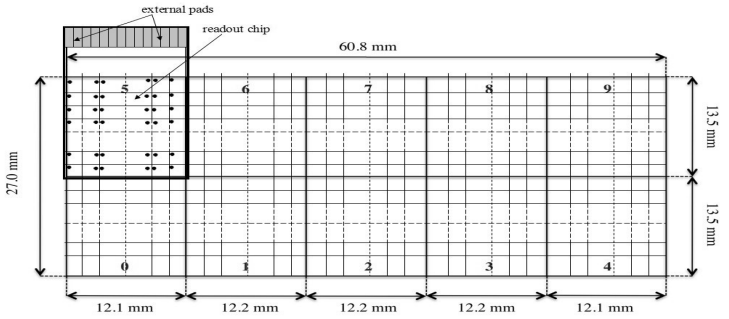

Figure 2. Readout chips

2. Readout architectures

Each readout chip, in the final version, will serve 1800 pixels. The total average data rate per chip it will be more than 4 Gb/s, which corresponds to a maximum of ~6 Gb/s with fluctuations. Due to the huge amount of data local buffering is not possible, therefore high speed serial links and a trigger less readout solution are necessary to be able to achieve the required efficiency of 99%.
To reach the required time resolution the compensation of the discriminator time-walk is mandatory. Time-walk problem can be addressed either via a Constant Fraction Discriminator (CFD) or a Time-Over-Threshold (TOT) correction. While the first approach requires only one measurement per hit, it poses more challenges on the design of the comparator. The precise time measurement required can be reached by either with a Time-to-Amplitude Converter based TDC serving a single pixel or via a bank of DLL-based TDC shared among several pixels. Preliminary investigations did not give a clear advantage of one solution over the other, therefore two prototypes, using the CMOS 130 nm technology, have been designed in order to have an experimental comparison of the performances.

2.1. *On-pixel TDC option*

In this architecture the time-walk correction is performed by a CFD filter and the time measurement is provided by a Time to Amplitude Converter (TAC) based on a Wilkinson ADC. Both CFD and TDC are implemented on each pixels cell (Figure 3).

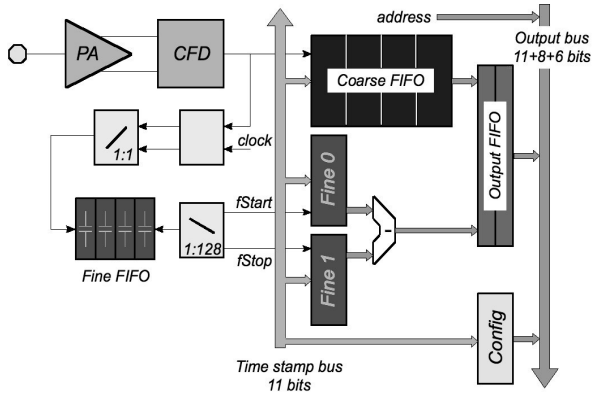

Figure 3. On-pixel TDC architecture: the pixel cell

The discriminated signal (CFD output) is used to store the value of the Time Stamp (11-bit bus), which gives the coarse time information with a granularity of 6.25 ns (160 MHz clock). The fine time information is provided by the TAC and the Wilkinson ADC, which give the time distance between the comparator output and the next clock rising edge. One of the advantages of this architecture is the derandomization performed directly on the pixel and the very low dead time which is only due to the ramp generator or in case of buffers overflow. The demonstrator chip is organized in two folded columns of 45 pixels and one smaller column with only 15 pixels (plus spare pixels for testing). For each of them a totally independent End-of-Column Controller is responsible to readout data, adding additional informations before to send them out via a serial shift register.

2.2. *End-of-Column TDC option*

In this architecture the discriminator time-walk correction is performed by the use of the Time Over Threshold technique. Each pixel cell drives a dedicated transmission line sending the discriminator output to the end of column block (Figure 4), where both the leading edge and the trailing edge are stored. The pulse width information is used to correct offline the time-walk, so the transmission lines have to be well calibrated in order not to degraded the timing information [3].

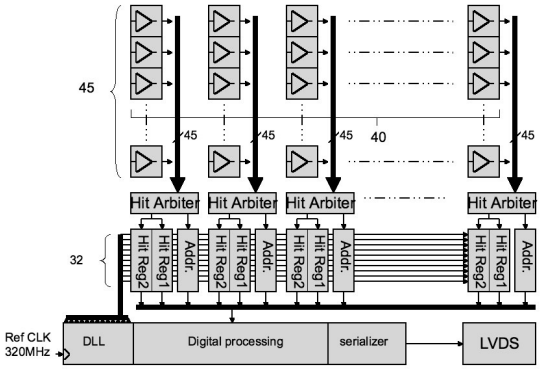

Figure 4. End-of-Column TDC architecture: global view

The precise time measurement is performed by a bank of DLL-based TDCs using a reference clock of 320 MHz. In this option a single TDC register is

shared among a group of 5 pixels. In order to have a low dead time the TDC must be very fast. In addition a hit arbiter should solve the ambiguities arising from two hits close-in-time in the same group of pixels.
The demonstrator ASIC has a whole 45 pixels folded column, with a single End-of-Column logic sending out the data by a serial shift register.

3. Summary

Both architectures offer advantages and disadvantages, so there is not *a priori* reason to use one solution over the other. The On-pixel TDC option has a major concentration of complexity in the pixel cell (power, noise due the digital circuits, radiation effects) but it is expected to have better performances in terms of dead time and amount of data produced. The second option (End-of-Column TDC) offers a simpler pixel cell but a more complicated system of transmission lines and a big concentration of digital noise sources at the End-of-Column (TDC banks, hit registers, decoders and counters). The two prototype ASIC have been produced and are currently being tested in order to evaluated which one is the best solution.

References

1. Letter of Intent to Measure the Rare Decay $K^+ \to \pi^+ \nu \bar{\nu}$ at CERN SPS. CERN-SPSC-2004-029 SPSC-I-229 (2004) .
2. M. Fiorini *et al.,*The P326 (NA48/3) Gigatracker: Requirements and design concept, *Nucl. Instr. and Meth.*, **A572**, 290 (2007).
3. A. Kluge *et al.,* An ultra fast 100 ps, 100 μm 3D-pixel imager. Proceedings of the 2008 SPIE conference. Volume **7249**, 724909 (2009).