The Gigatracker: an ultra-fast and low-mass silicon pixel detector for the NA62 experiment

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Abstract

The Gigatracker is a hybrid silicon pixel detector developed to track the highly intense NA62 hadron beam with a time resolution of 150 ps (rms). The beam spectrometer of the experiment is composed of three Gigatracker stations installed in vacuum in order to precisely measure momentum, time and direction of every traversing particle. Precise tracking demands a very low mass of the detector assembly (less than 0.5% X_0 per station) in order to limit multiple scattering and beam hadronic interactions. The high rate and especially the high timing precision requirements are very demanding: two R&D options are ongoing and the corresponding prototype read-out chips have been recently designed and produced in 0.13 μm CMOS technology. One solution makes use of a constant fraction discriminator and on-pixel analogue-based time-to-digital-converter (TDC); the other comprises a delay-locked loop based TDC placed at the end of each pixel column and a time-over-threshold discriminator with time-walk correction technique. The current status of the R&D program is overviewed and results from the prototype read-out chips test are presented.

Key words:
Solid-state detectors, Tracking and position-sensitive detectors, Silicon pixel ASIC, Time-to-Digital Converter

1. Introduction

NA62 is a fixed target experiment at the CERN SPS that aims at measuring $O(100)$ events of the ultra-rare decay $K^+ \to \pi^+ \nu\bar{\nu}$ with low background (~10%) in about two years of data taking [1]. The branching ratio of this decay is predicted with high accuracy within the Standard Model: a recent calculation yields $(8.5 \pm 0.7) \times 10^{-11}$, where the uncertainty is dominated by the CKM elements, as reported in [2] and references therein. Background reduction will be achieved by means of highly efficient photon vetoes and particle identification detectors, together with kinematical selections based on the missing mass variable:

$$m^2_{miss} \simeq m^2_K \cdot \left(1 - \frac{|p_\pi|}{|p_K|}\right) + m^2_\pi \cdot \left(1 - \frac{|p_K|}{|p_\pi|}\right) - |p_K| \cdot |p_\pi| \cdot \theta^2_{\pi K}$$

where p_K (p_π) and m_K (m_π) are the kaon (pion) momentum and mass, respectively, and $\theta_{\pi K}$ is the angle between the two tracks.

The beam spectrometer of the experiment consists of three Gigatracker (GTK) stations installed in vacuum and measures beam particles momenta and angles thanks to the deflections imparted by a quadruplet of dipole magnets, as indicated in Fig 1. The spectrometer has to sustain a high and non-uniform beam rate of ~1.5 MHz/mm^2 in the center and 0.8-1.0 GHz in total, hence the detector name. It should also limit multiple scattering and hadronic interactions of the 75 GeV/c beam particles: therefore material budget is minimized (0.5% X_0 per station or less) and the GTK stations will be installed in vacuum. The most demanding parameter of this detector is the time resolution of 150 ps (rms) for a single track, which will allow to associate the daughter pion track to the correct parent kaon.

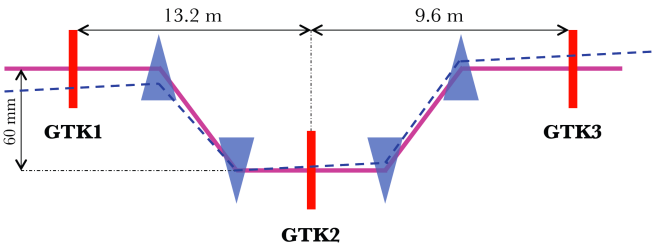

Figure 1: Schematic drawing of the NA62 beam spectrometer.

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2. The Gigatracker detector

A Gigatracker station consists of a single silicon sensor (60×27 mm^2) flip-chip bonded to ten read-out chips, as shown in Fig 2. A pixel size of 300 μm $\times$ 300 μm is sufficient to achieve the required momentum ($\sigma(p_K)/p_K \sim 0.2\%$) and angular ($\sigma(\theta_K) \sim 16$ μrad) resolution.

Sensor thickness has been fixed to 200 μm according to an optimization of the material budget and the signal-to-noise ratio required to achieve the target time resolution. The processing of high resistivity sensor wafers (p-in-n) started at FBK-irst (Trento, Italy) in summer 2009. In addition, to match the severe material budget requirements, the read-out chips will be thinned down to 100 μm or less.

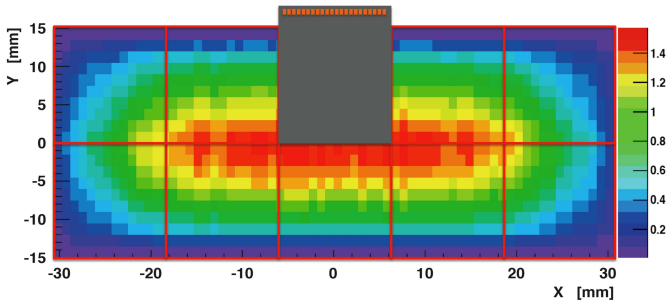

Figure 2: Beam intensity distribution over one GTK station (units are MHz/mm^2). A schematic drawing of one read-out chip is shown as well.

A fluence of up to 2×10^{14} 1-MeV n eq. cm^{-2} is expected in the central region of the sensor during one year of operation, a value which is comparable to the fluences expected for the LHC trackers over 10 years. Irradiation of p-in-n diodes with fast neutrons and protons have been performed, in addition to annealing measurements (I-V and C-V curves) following the expected run scenario, in order to characterize the sensor operation in a high radiation environment. Results show that the most critical parameter in operating the Gigatracker is the radiation induced leakage current, which can be kept to an acceptable value if the sensor temperature can be maintained below 5°C. The very low material budget for the detector, the necessary operation in vacuum and the harsh radiation environment demand a very efficient cooling system.

3. Cooling systems

Two cooling options with very low mass (~0.15% X_0 per GTK station) are currently under study. They should dissipate the total power produced by the read-out chips (~32 W per station) and keep the sensor at a stable and low temperature value.

One solution is based on convective cooling inside a vessel. As shown in Fig. 3, the detector is mounted on a printed circuit board (PCB) and housed inside a cylindrical aluminum vessel. The GTK assembly is separated from the vacuum by two thin (50 μm) kapton walls in the beam region and cooling is achieved through a flow of cold gaseous nitrogen (100 K at the inlet). A full size prototype has been built and is currently being tested.

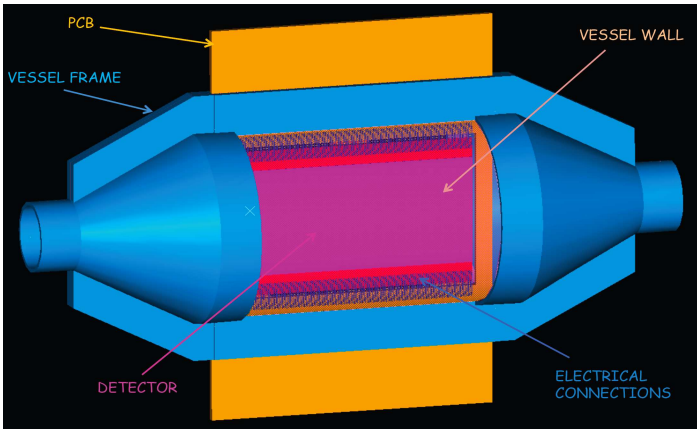

Figure 3: CAD drawing of the vessel cooling system. The kapton windows are not shown.

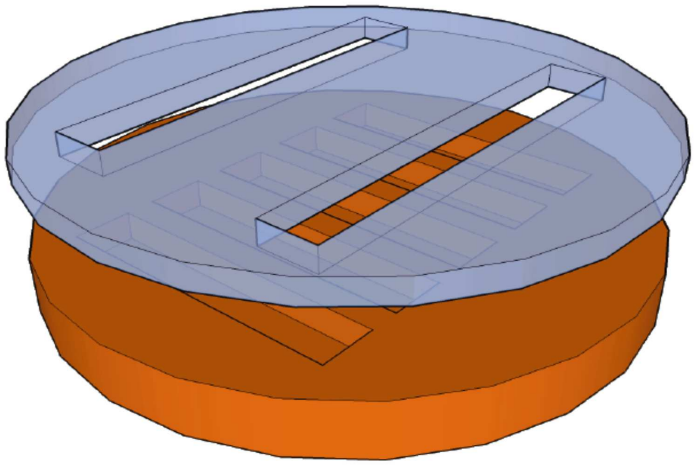

Figure 4: Schematic drawing of a micro-channel cooling plate.

The other option exploits conduction between the Gigatracker assembly and a micro-channel cooling plate, connected to it through a high thermal conductivity adhesive material. The cooling plate is composed of two silicon wafers bonded to each other, as shown in Fig. 4: 50 μm $\times$ 50 μm micro-channels are etched in the bottom wafer (100 μm total thickness) while openings for inlet and outlet manifolds are made in the top wafer (50 μm thick). A radiation-hard coolant (C_6F_{14}) will flow inside the channels to achieve the required heat dissipation. A first prototype based on silicon-Pyrex bonded wafers has been produced and a complete test stand is under construction.

4. Read-out architectures

The read-out chips will be produced in 0.13 μm CMOS technology: they comprise 40 columns of 45 pixels each (1800 pixels per chip in total) and are designed for a maximum rate of 140 kHz per pixel. Key challenges for the chip design are the time resolution (200 ps rms per single hit), the fast on-pixel analog pulse shaping (4 ns peaking time) and the high data rate per chip (up to 6 Gb/s).

Hit information will be sent directly out of the chip (triggerless architecture) to reduce the amount of data to be stored in the memory buffers of the chip. In addition, the hit detection efficiency of a single Gigatracker station should exceed 99%.

In order to achieve the required timing precision, time-walk compensation has to be applied due to the high dynamic range (5000 to 60000 electrons). Two complementary read-out architectures [3, 4, 5] have been implemented on small size prototypes to compare their relative performances.

4.1. On-pixel TDC option

This option measures, buffers, and digitizes the particle arrival time directly in each pixel cell and then transfers the digitized time-stamps to the periphery of the chip.

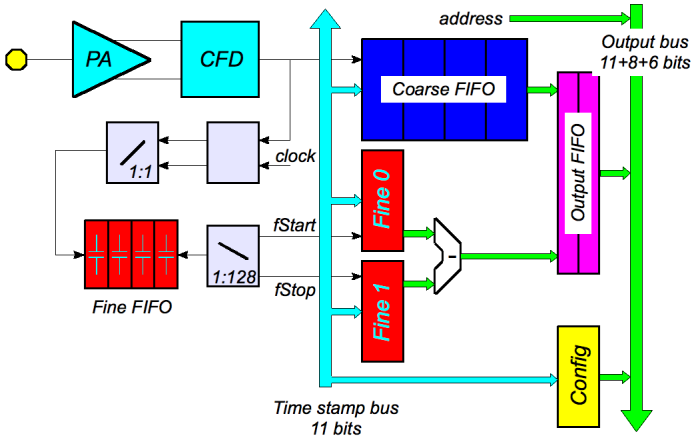

Figure 5: Schematic pixel cell diagram for the on-pixel TDC option.

Correction of the time-walk is achieved through a constant fraction discriminator (CFD), which measures the zero crossing time of the difference between the original input signal and a delayed and attenuated copy of the same signal. Depending on the proper optimization of the CFD parameters, the zero crossing gives the time at which the input signal reached maximum amplitude. When a hit is detected the content of the coarse bus (coarse time information) is latched into a digital buffer. In parallel the hit triggers a ramp generator to charge a capacitor. The charging-up is terminated by the semi-clock trailing edge: the voltage corresponds to the fine time measurement and is converted to a digital value by a Wilkinson ADC. The hit information (coarse time, fine time and pixel address) is stored into the output buffer before being transferred to the end-of-column logic. A schematic drawing of the pixel cell is shown in Fig. 5.

De-randomization is performed directly on the pixel cell: an analog pipeline stores time information inside the pixel cell before conversion in order to reduce dead-time in case of multiple hits. Simulations on the final system architecture have been performed in order to evaluate the FIFO depths and the number of lost events due to dead-time (less than 0.2% inefficiency at 140 kHz).

This approach requires only one time measurement per hit, while it poses challenges on the comparator design. A very low jitter clock signal (160 MHz reference frequency) must be sent to all pixels in the matrix: the separation of digital and analog domains is difficult, but each pixel acts independently. In addition, the pixel cell will be exposed to high levels of radiation and therefore must be designed to be radiation-hard in both total dose and single event upset (SEU) aspects.

4.2. End-of-Column TDC option

In this approach the analog front-end signals are discriminated inside the pixel cell and sent to the periphery of the pixel matrix, where the End-of-Column (EoC) circuitry performs the time measurement.

Two time measurements are performed for each hit (leading and trailing edges) and the time-over-threshold of the signal is used offline to correct for the time-walk. Hit arrival time is measured using a delay-locked loop (DLL) based TDC, which operates at a base frequency of 320 MHz (32 buffers divide the period of 3.125 ns into bins of 98 ps).

Several pixels can be multiplexed to one hit register: simulations show that a dead-time less than 0.5% can be achieved combining 5 pixels in a single hit register. Consequently 9 hit registers for the rising edge time and 9 hit registers for the falling edge time are used for each pixel column. A digital arbiter circuitry has been designed to send hit pulses to the TDC banks and block signals from the same group of 5 pixels in case they would overlap in time. These overlaps are flagged and the information is added to the output data stream. A schematic diagram of this architecture is shown in Fig 6.

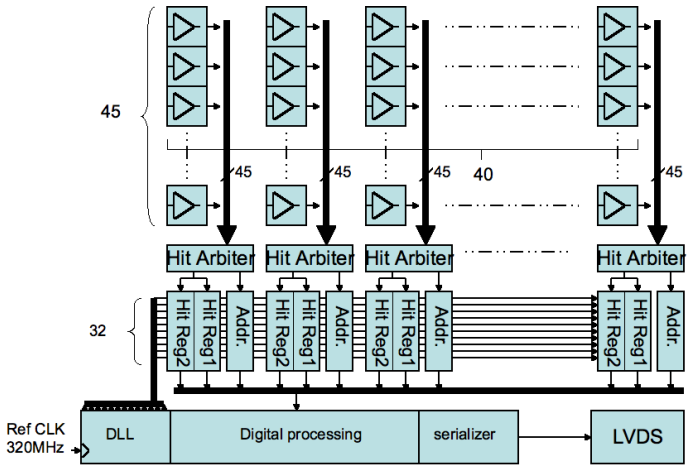

Figure 6: Schematic diagram of the end-of-column TDC architecture.

Compared to the on-pixel TDC architecture, processing inside the pixel cell is minimized in order to reduce noise to a minimum. However, the pixel comparator signals have to be propagated to the chip periphery and special techniques have been adopted to maintain the timing precision: each pixel output line is realized as a transmission line, driven in current mode, and pre-emphasis is implemented in the line driver.

4.3. Preliminary chip test results

Two small-area prototype chips, one for each architecture, were submitted in March 2009 to a Multi-Project Wafer run in

order to investigate and compare their relative performances. In summer 2009 the chips were delivered and tests started during the subsequent months.

The prototype chip for the on-pixel TDC option comprises 2 folded columns (45 pixels each) and one smaller column with 15 pixels, plus two test pixels, which will not be connected to the sensor. For each column a totally independent end-of-column controller is implemented, in addition to SEU protection both in the pixel cells and the end-of-column. Prototype tests are ongoing and results will soon be available.

The EoC TDC prototype chip contains 60 pixel cells divided into three groups: a main array with 45 pixels (folded full column) with 9 EoC read-out blocks, each one serving 5 pixels through the arbiter block; a small array with 9 pixels and a test array of 6 test pixels with analog output.

Qualification of the EoC prototype chip has been performed for both the analog front-end and the digital part. TDC performance characterization has been done obtaining stable operation of the DLL at a clock frequency of 250 MHz, which corresponds to a time binning of 125 ps (LSB). Both differential and integral rms non-linearities have been measured to be less than 0.2 LSB, while the bin width uniformity is ~0.15 LSB. The characterization of the analog front-end has been done exploiting the test pixel cells, which give access to the analog pixel output. An equivalent noise charge (ENC) of 56 electrons has been found. The time jitter of the discriminated pixel output has been measured to be less than 100 ps for an injected charge of ~3 fC, which corresponds to the mean charge released by minimum ionizing particles in the sensor.

Important measurements that have still to be done on the EoC prototype are full chain characterization, from the analog front-end to the TDC at the end of the column, and tests of the bump bonded assemblies with laser and particle beams.

Summary

The NA62 Gigatracker detector system and two prototype read-out architectures have been presented. The Gigatracker is a very challenging detector especially due to the time resolution requirement (150 ps rms for single track) and the high particle rate. Two solutions for a low mass cooling system (~0.15% X_0) are currently being developed to limit radiation induced leakage current and ensure stable detector operation. Two complementary read-out architectures have been designed and implemented as small area prototypes in 0.13 μm CMOS technology. Test results of one read-out chip are very promising.

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