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Characterisation Of The NA62 GigaTracker End of Column Demonstrator Hybrid Pixel Detector

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ABSTRACT: The architecture and characterisation of the NA62 GigaTracker End of Column Demonstrator Hybrid Pixel Detector (HPD) are presented. This detector must perform time stamping to 200 ps (RMS) or better, provide 300 μm pitch position information and operate with a dead time of 1 % or less for 800 $MHz-1\,GHz$ beam rate. The demonstrator HPD Assembly comprises a readout chip with a test column of 45 pixels, alongside other test structures, bump bonded to a p-in-n detector 200 μm in thickness. Validation of the performance of the HPD and the time-over-threshold timewalk compensation mechanism with both beam particles and a high precision laser system was performed and is presented. Confirmation of better than the required time stamping precision has been demonstrated and subsequent work on the design of the full-scale ASIC, dubbed TDCPix, is underway. An overview of the TDCPix architecure is given.

KEYWORDS: Pixelated detectors and associated VLSI electronics; Hybrid detectors; Timing detectors; Particle tracking detectors (Solid-state detectors).

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1. Introduction

NA62[1], a new fixed target experiment at the CERN Super Proton Synchrotron, aims to measure the ultra-rare decay of the positive kaon to a positive pion with a neutrino-antineutrino pair: $K^+ \rightarrow \pi^+ \nu\overline{\nu}$.

The GigaTracker[2] (GTK) hybrid pixel detector comprises three stations situated early in the beam decay line, designed to measure the momentum, angle and interaction time of the beam particles. The requirements on these parameters are driven by the demanding background rejection level necessary for the rare kaon decay measurement. In total, the beam rate incident on the GigaTracker is expected to be around $800\,MHz - 1\,GHz$, which equates to approximately $140\,kHz$ per pixel in the centre, where the intensity is the highest. The total dead time of the detector is required to be less than 1%. The radiation environment is expected to be extremely harsh, with the total fluence per year approximately $2\,\mathrm{x}\,10^{14}\,1\,MeV\,neq.yr^{-1}$: similar to that expected in 10 years of operation for a central tracking detector in an LHC experiment.

Each detector instruments an area of 60.8 *mm* x 27 *mm* and consists of an array of 18000 pixels, each one nominally 300 x 300 μm^2. Time stamping is required to the level of 150 *ps* (RMS) for the GTK as a whole and better than 200 *ps* (RMS) per station.

A demonstrator readout ASIC [3] and detector were designed and fabricated and have undergone extensive combined and independent electrical, laser and beam testing. Architecturally, this design is based on an asynchronously operating pixel matrix with a single threshold discriminator per pixel. Hit time stamping is done in the End of Column (EoC) region by a delay locked loop based time-to-digital converter, with the high precision timing signals from the discriminator being transferred to EoC by means of a dedicated, per-pixel, transmission line. A time over threshold

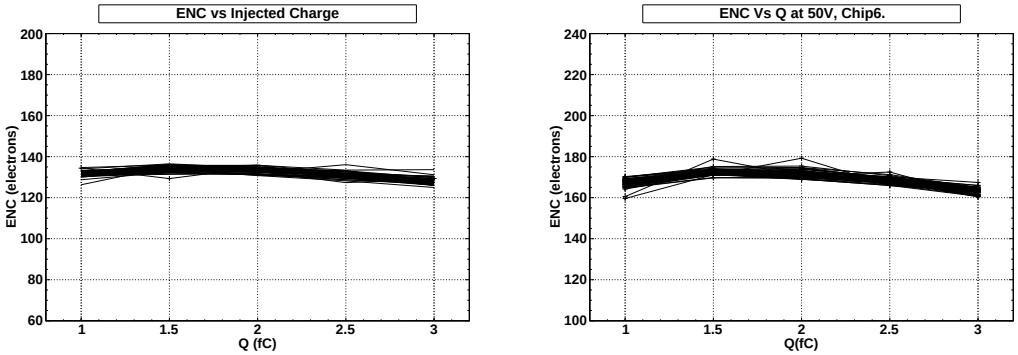
measurement, coupled with an off-detector look-up is used to effect the discriminator time walk correction.

Discrepancies between the time resolution measured with particles during the beam test and that measured in the lab with the laser system were significant and warranted investigation. A detailed study of the behaviour of the sensor and readout electronics was subsequently undertaken to identify and characterise these additional contributions to the timing resolution seen with particles. The demonstrator system exhibits a time-stamping resolution of better than 200 *ps* (RMS) per station for single particles.

2. Measured Performance

2.1 Noise

The noise of a pixel with a single discriminator output must be obtained indirectly by measuring the pulse height spectrum in the presence of a known and constant injected charge.



(a) No sensor.

(b) Fully depleted sensor.

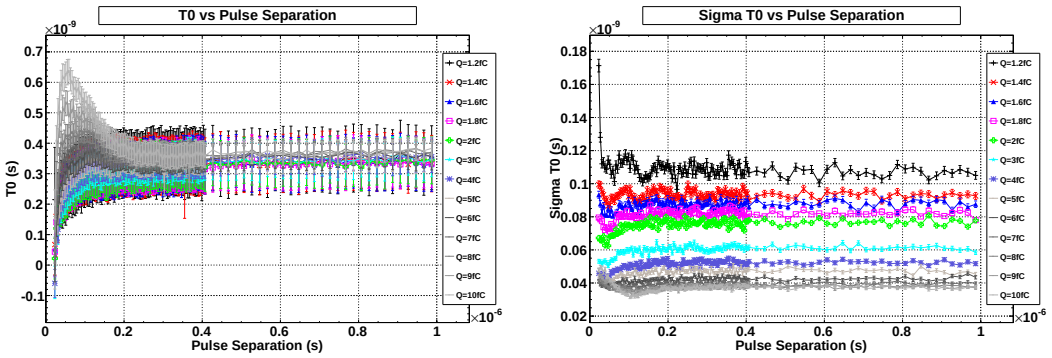
Figure 1. ENC as a function of injected charge with and without sensor present.

A fixed charge is injected into the pixel a reasonably large number of times (10000 in this case), and the discriminator response count is recorded as a function of the discriminator threshold. This turn-on curve represents the cumulative frequency of the pulse height spectrum. Fitting the curve with the error function reveals the properties of the underlying Gaussian (width and mean). Repeating this procedure for several charges in the linear range of the preamplifier also permits the gain and offset to be extracted, and from these the noise (standard deviation) may be referred to the input to yield the equivalent noise charge (ENC). Figure 1 shows the result of such a measurement across all 45 pixels in the main array of two distinct readout ASICs one bare, the other with a sensor bump bonded and biased comfortably over full depletion. The noise figures obtained here are at a better than acceptable level for the correct operation of the circuit.

2.2 Pulse Separation Studies

Due to the high rates expected in the GTK, it is important to understand the behaviour of the pixel when two pulses are close together: specifically how the second pulse might be disturbed due to the presence of the first pulse. To investigate this situation, a high precision infra-red laser was

used to inject charge into the centre of the test pixel with a controllable time between neighbouring pulses. The average rate of the pulse generation was kept constant at 200 kHz, whilst the pulse separation was varied from 20 ns to 1 μs. The discriminator output was digitised using a fast real-time oscilloscope, and a nominal 0.7 fC threshold was set in the pixel.



(a) Reconstructed Time

(b) Reconstructed Time Jitter

Figure 2. Test pixel and time walk correction behaviour as a function of pulse separation.

A correction look-up table was populated, permitting the charge-independent event time to be extracted for the second pulse in the pair. This reconstructed time is shown in figure 2 (a) as a function of pulse separation for injected charges from 1.2 - 10 fC. Note that both the aggressor pulse and pulse under study have the same charge as each other. The reconstructed time remains constant above pulse separations of approximately 200 ns, below this, a systematic deviation from the expected flat line is observed. This can be understood by considering the undershoot after the aggressor pulse as causing a systematic shift in the baseline relative to the threshold for the second pulse in the pair. This causes a corresponding change in the time over threshold, and hence an error is introduced in the time-walk corrected time.

Figure 2 (b) shows the jitter of this corrected time as a function of pulse separation over the same charge range. The behaviour is largely flat with some deviations at small separations. The first of these occurs at very small separations for the smallest charge and is due to the discriminator approaching the pulse peak. Otherwise a systematic improvement of the jitter performance can be seen typically below 100 ns for charges above about 2 fC. This improvement is due the effective decrease of the baseline moving the discriminator crossing point up the leading edge of the pre-amplifier output to a steeper part of the pulse. This increase of the gradient at the crossing provides a shorter lever arm into the time domain for the noise on the pre-amplifier output, and hence the improvement. Notably, for the 10 fC charge, this improvement begins to disappear as the separation drops below 100 ns. This is understood as the second pulse walking up the back side of the aggressor pulse, thus redressing the suppression of the baseline and returning the effective threshold to what it was before.

As this effect is systematic, recording the time and time over threshold of the aggressor pulse will permit second order corrections to be applied to the time over threshold correction.

2.3 Transmission Line Performance

It was necessary to validate the architectural choice to transfer the high precision timing signals from the pixel to the end of column region. The detector dimensions necessitate that this approach perform adequately for a minimum length of 13.5 mm (45 pixels * 300 μm) for the farthest pixel.

In reality some additional length will be required to traverse column resources to be abutted to the end of the column.

Figure 3 shows the discriminator jitter as a function of pixel distance from the EoC region along the whole length of the column for representative charges from 1 - 10 fC.

There is no observable systematic degradation of performance as a function of this distance. The distance shown here includes the additional length required to orchestrate the folding of the column, needed to realise the demonstrator ASICs with an acceptable form factor. The jitter values for each pixel and charge are averaged over the phase of the charge injection relative to the clock signal, which is swept through the full clock period in 314 steps of 10 ps.

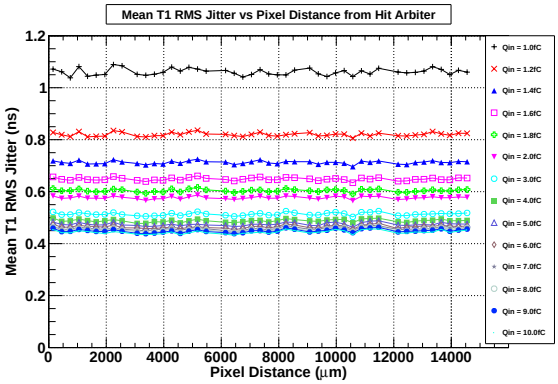
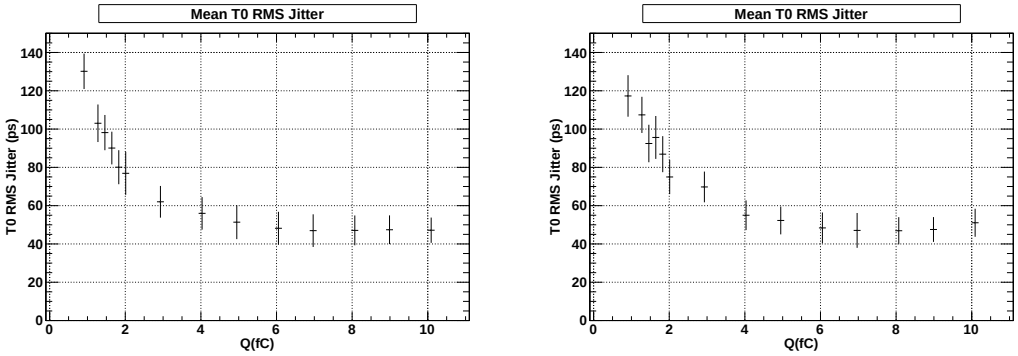


Figure 3. Mean discriminator jitter as a function of pixel distance from the EoC.

2.4 Full Chain Detector Performance

Performance of the full chain from detector to TDC, including the time walk correction was measured using the infra-red laser shone into the pixel centre. The phase of the charge injection was varied across the full clock period in 314 steps of 10 ps, from 0 to 3130 ps.



(a) Pixel 0: far from EoC

(b) Pixel 44: close to EoC

Figure 4. Jitter of time-walk corrected time as a function of injected charge.

A separate calibration data set was used to fill the look-up table to effect the time walk correction, thus keeping the calibration and the measurement statistically independent. At least 10000 samples per charge were acquired in each set. Figures 4 (a) and 4 (b) show the mean full chain jitter performance as a function of charge over the range 1 - 10 fC for the far and near pixels respectively. In both cases, the discriminator threshold was set to 0.7 fC and the detector was biased at 300 V. The vertical uncertainties represent the distribution of the jitter due to the phase of the signal relative to the clock. These plots show that there is no significant feed-through from the digital activity in the EoC region to the pixel closest to it. At the most probable charge of 2.4 fC, the RMS timing resolution is approximately 75 ps.

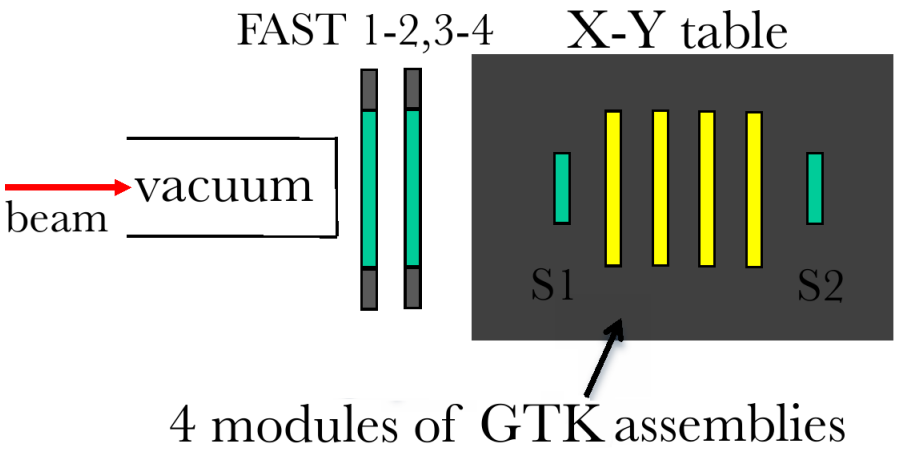


Figure 5. Schematic of the setup for the CERN PS beam test.

2.5 Beam Test Performance

In September 2010 four assemblies were aligned and placed in a 10 GeV beam, comprising mainly pions and protons, at the CERN PS. Peripheral to the assemblies were some trigger scintillators aligned to the assemblies and some fast timing reference scintillators with double-ended PMT readouts. The time-stamping of hits from these scintillators was done with the CAEN V1290A [4]. Figure 5 shows a schematic representation of the key components placed in the beam. The GTK planes are shown in the centre of

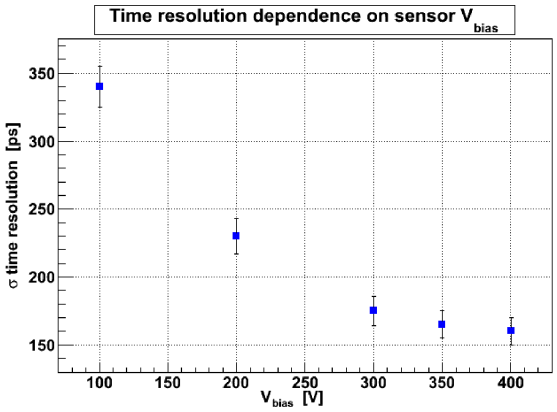


Figure 6. Time resolution across all pixels of one GTK plane as a function of sensor bias.

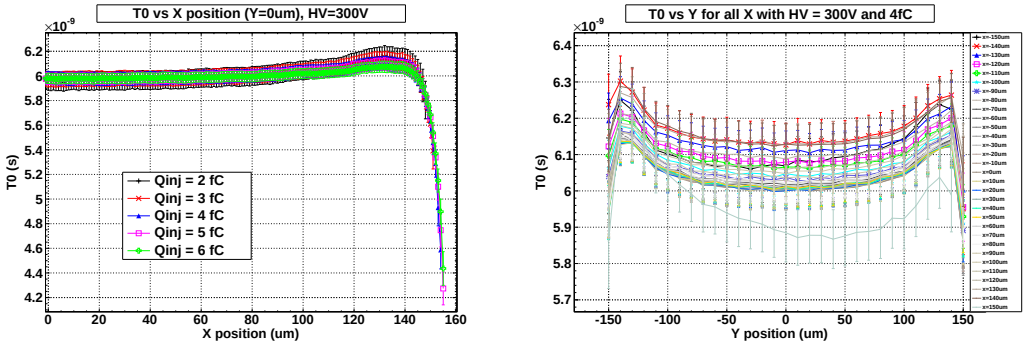
the X-Y table, used for beam alignment, as yellow planes. The trigger scintillators are labeled S1 and S2, and the timing reference scintillators are labeled FAST 1-2,3-4.

Figure 6 summarises the average measured performance across all pixels of a GTK assembly with beam particles as a function of the detector bias at values from $100\,V$ to $400\,V$. At the nominal $300\,V$ bias, the average time resolution is approximately $175\,ps$. Note that the spread of performance includes in it variations of the effective discriminator threshold, since in-pixel threshold trimming is not possible in the demonstrator ASIC.

2.6 Pixel Geometrical Studies

This result alone is important demonstrating that the approach investigated here provides sufficient time-stamping performance for the GTK application. However, there remains a significant difference between this and the resolution that might be expected given the experimental results obtained through measurements with laser charge injection into the similarly biased detector. The most immediately obvious differences are that the charge release mechanisms are different and that the particle beam illuminates the pixel uniformly in its lateral extent. The latter of these issues has been directly investigated by sweeping the laser spot across the pixel and recording the discriminator response over a range of charges. The results shown here are for the nominal $300\,V$ sensor bias.

Figure 7 (a) shows the reconstructed time scan from 0 to $154\,\mu m$ (i.e. from the test pixel centre to the edge) along the centre line of the pixel in steps of $2\,\mu m$ for charges 2, 3, 4, 5 and $6\,fC$. The deviation from the expected flat line is clear and becomes significant as the edge of the pixel is reached and exceeded.

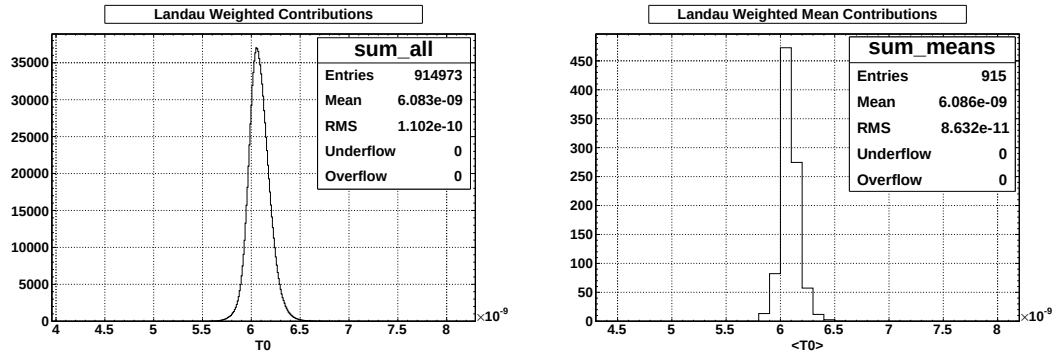


(a) A $2\,\mu m$ step scan along the pixel centre line from the centre to the edge for charges 2-6 fC.

(b) A $10\,\mu m$ step scan across the whole pixel for charge of $4\,fC$.

Figure 7. Reconstructed time as a function of position within the pixel.

A second series of scans was done across the full pixel in X and Y over the same charge range. A step size of $10\,\mu m$ was used in the measurement in order for it to complete in a timely manner. Figure 7 (b) shows the behaviour of the reconstructed time summarised as a function of Y for each X, for the charge of $4\,fC$. The systematic error in the reconstructed time is clearly present in both directions as the edge of the pixel is approached. In both sets of measurements, 1000 samples per position were acquired. An independent calibration scan was made to provide the look-up table for the correction.



(a) All contributions.

(b) Systematic contributions.

Figure 8. Laundau weighted distribution of the reconstructed time over the whole pixel.

To estimate the effect that this systematic shift has on the timing resolution of the system, the summary histograms shown in figures 8 (a) and (b) were made. The first is a Landau weighted sum of histograms filled for each charge from the X-Y data set. Here, all samples where the discriminator fired were included. This histogram has a standard deviation of approximately 110 *ps*, which includes both the stochastic component and the broadening seen from the error in the correction. The second histogram, shown in 8 (b) contains just the Landau weighted mean values for each X-Y point, and exhibits a standard deviation of approximately 85 *ps*. Subtracting this width from the total width in 8 (a) in quadrature should yield the stochastic component, and indeed a value of approximately 70 *ps* is found.

The reason for this variation originates from the weighting potential: modification of the induced current in the charge collection electrode as a result of the geometry of the pixel. The shape of the current pulse seen by the front end is thusly dependent on the position of the charge injection. This in turn modifies the shape of the preamplifier output which distorts the discriminator events. As it is not possible to provide sub-pixel position information, the variation causes a degradation of the timing performance.

3. Scaling Up the Design Concept: TDCPix

The design concept investigated through this demonstrator system is being scaled up to a full size ASIC comprising 40 columns, each with a full complement of 45 pixels. A diagram showing this is presented in figure 9. The columns in the chip are organised into pairs, with each pair sharing the column services. The transmission lines for the 90 pixels in a column pair run down the centre of the pixels and the column services to the EoC region for time-stamping.

Some of the services required by the column pair are the discriminator thresholds, transmission line bias trim, calibration pulse generation and configuration, and an analogue multiplexer that will enable the on-chip DACs to be calibrated. All parameters in the column pair are controlled through a bus that runs up the left hand side, and down the right hand side. The configuration blocks are arranged such that they abut end-to-end to facilitate the routing of the control signals.

The TDC[5] is situated below the column services at the end of the transmission lines. It is a multi-stage design comprising a DLL with 32 contributing delay cells to give sub-clock cycle

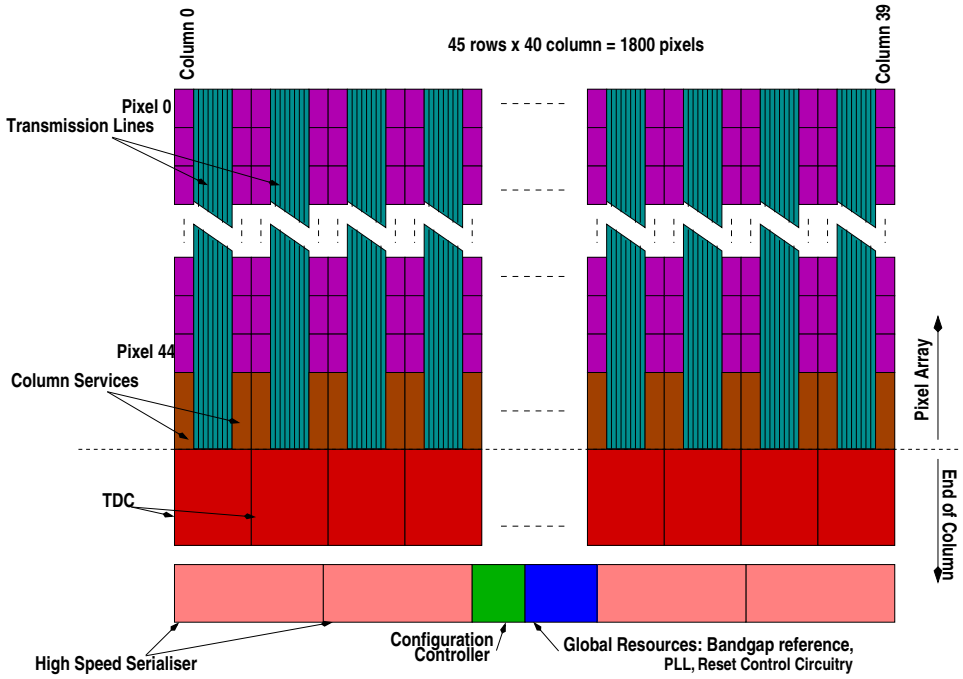


Figure 9. A top level schematic of the main components in the TDCPix design.

precision with some range-extending counters and a series of hit registers into which the state of the delay line and coarse counter are latched upon the receipt of a hit. Hits are buffered with a FIFO per channel and the data streams are merged with a multiplexer before a final buffering stage. Each column has a dedicated set of hit registers and buffers, though the DLL and the start-up state machine are shared between two columns.

TDCPix possesses four high speed serialisers, each one charged with the task of reading out the data from a quarter of the device. Thus a quarter chip sees the input from 10 columns. A multiplexer at the input to the quarter chip merges hits from the column output into a larger FIFO before serialisation takes place. There is a frame generation system to mark the coarse counter rollover and communicate other status information to the data recipient. Additionally, some test patterns are foreseen.

A single configuration controller is present in the chip. This receives and replies to control commands via a full duplex link with one input and one output line. All internal configuration parameters and status signals will be set up and monitored via commands sent through this interface. Other global resources include, but are not limited to, digital and analogue band-gap references, a phase locked loop, reset management circuitry, and temperature surveillance. These components are beyond the scope of this paper and will be the subject of a future publication.

4. Conclusions

A demonstrator ASIC and detector hybrid were designed, fabricated and have undergone extensive testing. The performance requirements are dictated by the NA62 experiment, and are extremely stringent with regards to the timing performance, which must be better than 200 ps per station,

amongst others. The demonstrator ASIC architecture centres around an asynchronously operating pixel matrix with transmission lines to carry the high precision discriminator signals to the end of column region. In this manner, there is no distribution of high precision clock or time stamp codes throughout the matrix. The TDC is a multi-stage design, based on a DLL for sub-clock cycle precision and a pair of counters to extend the dynamic range with a nominal bin size of 100 ps. Characterisation results pertaining to the bare ASIC may be found in reference [3].

The ASIC was bump-bonded to a 200 μm thick p-in-n sensor and extensive characterisation of the combined entity has been done through the use of electronic charge injection, a high precision infra-red laser and a beam test. The performance of the sensor when stimulated with the laser remains in line with expectation and a timing resolution of approximately 75 ps is seen at the most probable charge.

The transmission line approach is shown not to degrade the timing performance of the system as a function of the distance from the EoC region. Additionally, the pixel is shown to operate very well in the presence of a higher than anticipated hit rate (200 kHz average) with hits as close as 20 ns apart.

The beam test showed that for single particles under nominal bias conditions the demonstrator system was capable of achieving a mean time stamping precision of approximately 175 ps.

Subsequent investigation with a high precision focused infra-red laser showed a clear dependence of the reconstructed time on the position of the charge injection. This was identified as being due to the weighting field. The magnitude of the effect was characterised and, although a significant contribution, there remains one or more other effects. Currently investigations into how inhomogeneities in the charged pair generation might effect the timing are underway.

At present, our team is engaged in the development of the full-scale ASIC. This represents the scaling up of the EoC concept into a 1800 pixel version.

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