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TEL62: an integrated trigger and data acquisition board

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ABSTRACT: The main goal of the NA62 experiment at the CERN SPS is to measure the branching ratio of the ultra-rare $K^+ \to \pi^+ \nu\nu$ decay, collecting about 100 events in two years of data taking. The experiment puts stringent requirements on the trigger and data acquisition system: the efficient online selection of interesting events and loss-less readout at high rate will be key issues. Readout uniformity of sub-detectors and scalability were taken into account in the architecture design. For this purpose an integrated trigger and data acquisition board (TEL62) was designed; the first prototype is currently under test.

KEYWORDS: Trigger concepts and systems (hardware and software); Data acquisition circuits; Data acquisition concepts; Digital electronic circuits

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1 Introduction

The NA62 experiment at the CERN SPS [1] aims at measuring the kaon decay $K^+ \to \pi^+ \nu\nu$ as a highly sensitive test of the Standard Model (SM) and a search for New Physics. The detection of this process is very difficult due to the smallness of the signal and the presence of a very sizeable background. Efficient online selection of candidate events and vetoing of background represents a very important issue for this experiment, because of the large rate reduction required before recording events on tape. A common general-purpose integrated trigger and data acquisition board (TEL62) was designed and is described in the following.

2 The NA62 experiment

The ultra-rare decay $K^+ \to \pi^+ \nu\nu$ is an excellent precision probe of the SM because of its remarkably clean nature from a theoretical point of view. Thanks to strong suppressions, the process is dominated by short-distance physics, which can be reliably computed, making it very sensitive to the possible existence of new particles, complementary to direct searches at the LHC and potentially sensitive to much higher energy scales. The predicted branching ratio [2] is very small $(7.80 \pm 0.85) \cdot 10^{-11}$, and the decay is at present very poorly measured, with only 7 candidate events detected in two dedicated experiments at Brookhaven [3].

NA62 aims to collect about 100 signal events in about 2 years of data. To this purpose, at least 10^{13} K^+ decays are estimated to be required. Rejection factors of the order of 10^{12} and the possibility to measure efficiencies and background suppression factors directly from data are mandatory.

The use of a high-energy (65 GeV/c) decay-in-flight technique in NA62 matches well the characteristics of the CERN SPS, helps in background rejection and sets the longitudinal dimensions of the experiment, with sub-detectors spread over more an area more than 100 m long. The rate in each of the main sub-detectors is about 10 MHz.

A schematic layout of the experiment is shown in figure 1, in which the 65 m long fiducial decay region is visible, together with tracking and particle identification devices for both K+

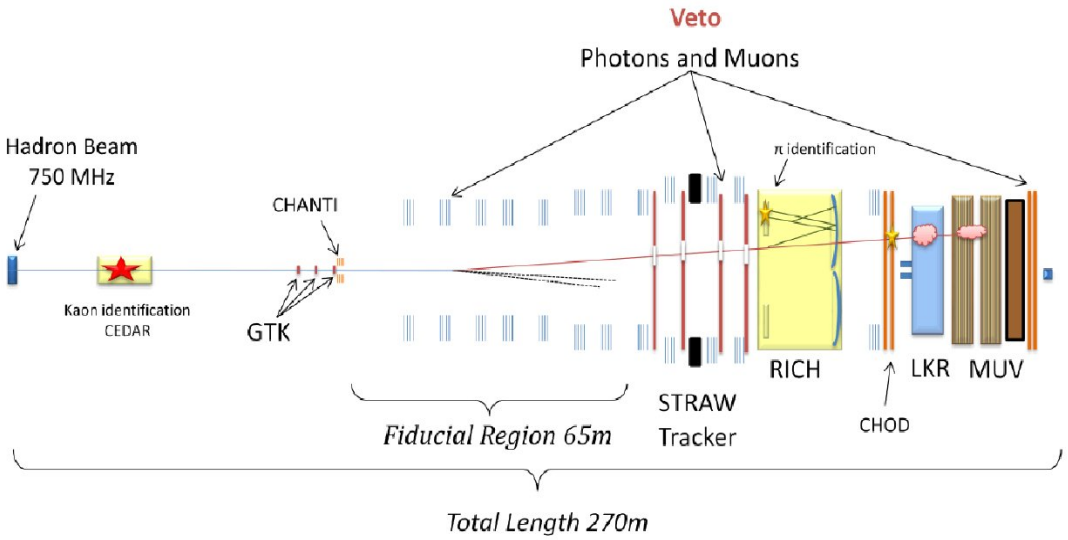

Figure 1. Schematic view of the NA62 experiment, showing the main sub-detectors.

(GTK, CEDAR) and π+ (STRAW, RICH) and vetos for photons, positrons and muons. A scintillator hodoscope (CHOD) acts as a fast timing and trigger device, together with veto sub-detectors (LAV, LKR, MUV).

3 The Trigger and DAQ system

The intense flux of a rare decay experiment, such as NA62, where the rate of the events in the decay region is strongly dominated by background, requires high-performance triggering and data acquisition. These systems must minimize dead time while maximizing data collection reliability. A unified Trigger and Data AcQuisition (TDAQ) system [6] was designed, which assembles trigger information from readout-ready digitized data in a simple cost-effective way. For most sub-detectors in NA62 the building block of this system will be the TEL62 board.

A common phase-coherent clock, with a frequency of approximately 40 MHz, generated centrally by a single free-running high-stability oscillator, will be distributed optically to all systems through the Timing Trigger and Control (TTC) system designed and used in LHC experiments [4]. NA62 will have a hardware lowest-level trigger (Level 0, L0) working on digitized sub-detector data. Following a L0 trigger, most sub-detectors will transfer data corresponding to a programmable time window from TEL62 boards (through Gigabit Ethernet links) to a PC farm, where two further software trigger levels will be implemented, L1 before and L2 after event-building (see figure 2).

The single hardware L0 trigger will reduce the total rate from 10 to $\sim$1 MHz using information coming from the charged hodoscope (CHOD), RICH, Large Angle Veto (LAV), Liquid Krypton (LKr) calorimeter and Muon Veto (MUV) detectors. The default (primary trigger) algorithm will be implemented to collect events with a single track in the CHOD, nothing in the MUV, and not more than one cluster in the LKr. The inclusion of other sub-detector information is possible, both

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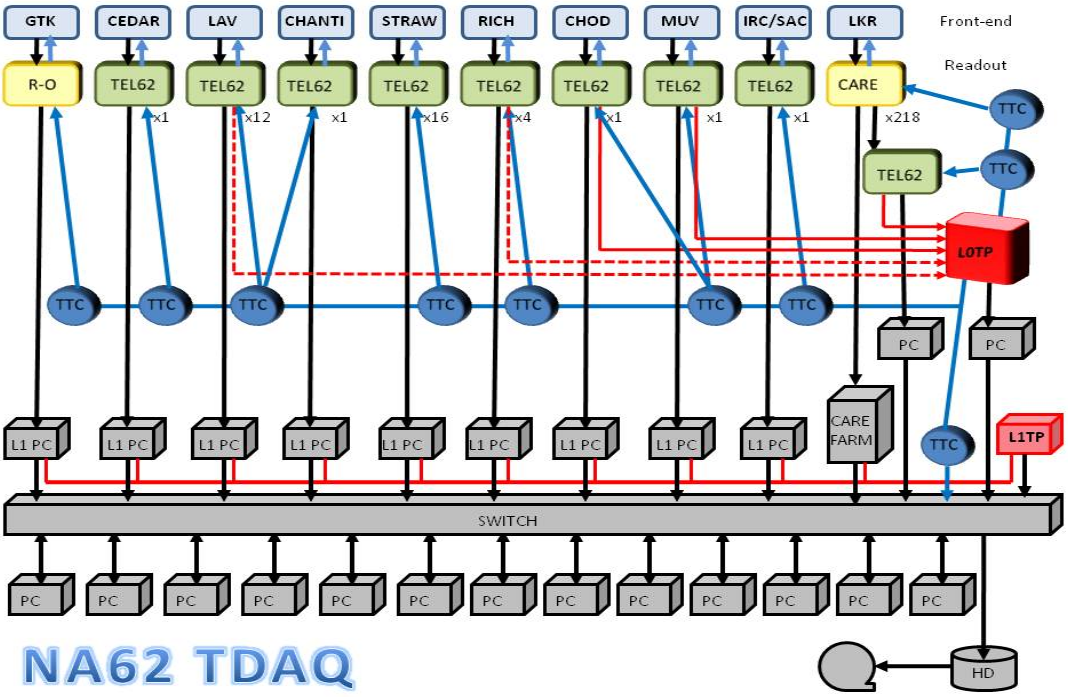

Figure 2. Schematics of the NA62 trigger and DAQ system.

to refine the primary trigger and to implement secondary triggers for control samples and different physics goals. Data from all sub-detectors will be stored in front-end buffers (such as those hosted on the TEL62) during L0 trigger evaluation. The L0 latency is constant and required to be below 1 ms. The L0 trigger is transmitted to the TEL62 boards by the TTC system, together with a precise timestamp (25 ns resolution). Upon reception of a positive L0 trigger, most sub-detectors will send their data to dedicated PCs within an adequate time window around a L0 timestamp. The minimum window length is 75 ns, and will be optimized during the run. For each L0 trigger, all centrally-enabled sub-detectors will respond by sending a data frame. The type and amount of data it contains may be different for different trigger types; a data frame may even be empty or indicate an error. No sub-detector may ignore a L0 trigger.

4 TEL62 architecture

The TEL62 board (see figure 3) is a major upgrade of the TELL1 board designed by EPFL Lausanne for the LHCb experiment at CERN [5]. The design has a similar overall architecture, but the board is based on much more powerful and modern devices, resulting in more than four times the computational power and more than twenty times the buffer memory of the original, plus several other improvements in terms of connectivity.

The TEL62 will handle both the data and L0 trigger primitives flow.

Referring to figure 3 and figure 4, one should note the following parts:

1. 4 FPGAs (Pre-Processing or "PP") are Altera StratixIII (EP3SL110F1152C4N). Each one is

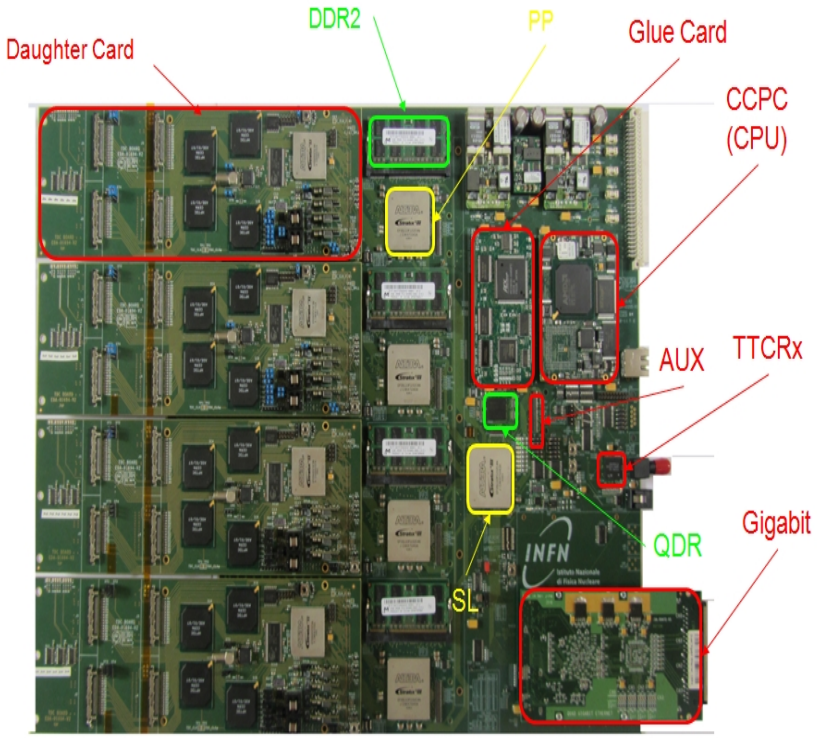

Figure 3. TEL62 with TDC daughter cards plugged in.

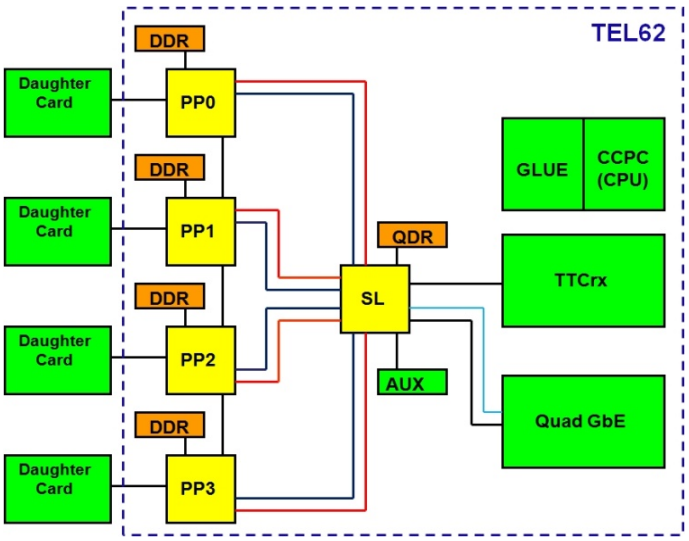

Figure 4. TEL62 architecture.

connected to a mezzanine card (in particular newly designed TDC Boards) through a 200-pin connector, and also to 2-GByte DDR2 memory buffers (SODimm form factor) which store the data during the L0 trigger latency.

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2. The central FPGA (SyncLink or "SL") is also an Altera StratixIII of the same type. Each PP is connected to the SL through two independent 32-bit data buses reserved for data and L0 trigger primitive flow. Each bus runs at 120 MHz and all signal lines have been properly terminated and equalized in length to handle this speed. The SL is also connected to the output mezzanine through another high-speed bus. The data and L0 trigger primitives from all PP are linked, possibly zero suppressed and encapsulated on the SL, where aggregation with data from other TEL62 boards can also take place. The data from several events is packed in a Multi-Event Packet and stored in an external buffer based on a Quad Data Rate (QDR) Synchronous Pipelined Burst SRAM, and finally sent to the output board. The chosen high-bandwidth dual port QDR device allows simultaneous read and write operations. With a bus width of 16-bit at double data rate and 100 MHz clock frequency, a bandwidth of 3.2 Gbit/s is reached. The chosen QDR memory chip (K7Q161852A-16) provides a depth of 1 MByte and is the smallest available.

3. The TDC Board ("TDCB") is a custom mezzanine equipped with 4 High Performance Time to Digital Converter (HPTDC) chips [7] a controller FPGA and 2 MB of static RAM. The board will service 128 sub-detector channels (LVDS) over 4 halogen-free SCSI-3 twisted-pair cables, measuring time and time-over-threshold with 100 ps LSB precision. Some capability to process data will be built-in. Up to 4 boards can be housed on a TEL62, for a total of 512 channels per mother-board. When TEL62 is equipped with TDC boards, two slots of crate space per mother-board are required.

4. The output board is a custom mezzanine, "Quad-GbE" (identical to the one on the TELL1) which implements 4×1 Gbit copper Ethernet channels used to connect the TEL62 board to the central L0 Trigger Processor (L0TP), and possibly to other TEL62 boards in a daisy-chain configuration, and also to send the main readout data to the DAQ farm.

5. The slow control, monitoring and configuration of the board is handled by 2 more mezzanines: a commercial Credit-Card PC (CCPC) running Linux and a custom input/output interface card (Glue Card[1]) connected to the CCPC through a PCI bus. Three different communication protocols are implemented on the Glue Card and distributed to all devices and connectors on the TEL62: JTAG, I2C and ECS. The JTAG is used to remotely configure all the devices on the board, I2C is mainly used to set registers on the TDCB cards, while ECS is a custom bus used to quickly access the TEL62 FPGAs internal registers.

6. The clock of the system and the L0 trigger information are distributed to all the TEL62 boards through a CERN-standard optical TTC link. The TEL62 uses a TTC receiver chip (TTCRx) [8] to decode clock and trigger information.

7. The FPGA configuration data is stored in two 64 Mbits EEPROMs. The 4 PP FPGAs are programmed with the same code.

[1] Designed and built by INFN Genova for LHCb.

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8. Dedicated connectors on the board allow daisy chaining of several TEL62 boards, in order to collect L0 trigger primitive data from all the boards of a single sub-detector without giving up two of the Quad Gbit links.

The board size complies with the 9U Eurocard standard. The printed circuit is made of 16 layers, with all lines controlled in impedance (50 Ohm). Special care has been used to route the clock tree, to avoid signal jitter as much as possible.

The power from the crate is distributed over a custom power backplane. The used voltages and the absorbed currents (with 4 TDCB plugged in) are:

Digital 5V: 1A

Digital 48V: 0.5A

Digital 3.3V: 2A

Analog –5V: 0A

Analog +5V: 3A

The overall power consumption is around 50W per TEL62 board.

The firmware for the FPGAs is currently under development within a common distributed framework (Mentor Graphics HDL Designer© and Altera Quartus II©). In the block diagrams of figure 5 a Data Flow and a L0 Primitive Trigger Flow can be identified.

Data Flow:

1. PPs receive data from the TDCB mezzanines, currently packed in 12.8 μs time frames.

2. On the fly monitoring of the data is performed in order to detect errors, which are recorded and signaled to the Data Acquisition supervision system at the end of each beam spill (about once per minute).

3. The DDR2 memory space is segmented in the firmware so that data corresponding to small time slots (currently 25 ns wide) is stored in dedicated memory areas. Each word received by the TDCBs is written into the first empty address of the space reserved to the time slot.

4. For each time slot a counter is incremented every time a word is written (the same counter is used as address generator for the LSB memory address bits).

5. When a L0 trigger reaches the SL it is time-stamped and distributed to all PPs, where the data for relevant time slots is read from the DDR2, packed and sent to the SL.

6. The SL merges all the received data and sends it to the PC farm through dedicated links on the Quad-GbE card.

L0 Trigger Primitive flow:

1. PPs receive data from the TDCB mezzanine.

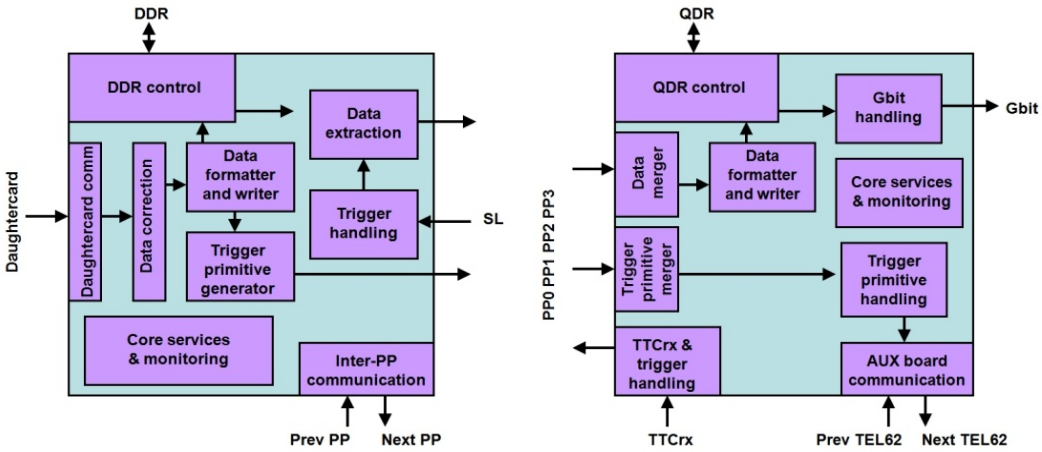

Figure 5. PP and SL firmware block diagrams.

2. Part of the data is processed on the fly to generate L0 trigger primitives; this is different for each specific sub-detector, and involves data adjustments (e.g. calibrations) and analysis. As an example, for the RICH sub-detector counters associated to each 25 ns time slot are defined and incremented by words received from the TDCB to build hit multiplicity information, and a primitive is generated whenever this quantity exceeds a given threshold for a time slot, indicating that a potentially interesting event is contained in it; the multiplicity count and time are sent to the SL whenever such condition is detected.

3. The SL collects trigger primitives and possibly merges them with those from other TEL62 boards, finally sending a trigger packet to the L0 Trigger Processor through a dedicated Gbit Ethernet link. Such processor, currently under design, collects all timestamped primitives and applies an appropriate algorithm to decide if a L0 trigger should be generated to read the event related to a certain time slot from all readout cards. In case of a positive decision such trigger is sent to all the TEL62 as a synchronous pulse on the TTC link followed by some trigger information.

5 Conclusions

The first prototype of the integrated TEL62 Trigger and Data Acquisition board is currently under test; a first pre-production is foreseen in the coming months for the first integration and data-taking tests of the experiment, occurring in 2012. The final production of about 80 boards plus spares is expected in 2013 for the NA62 experiment.

References

[1] NA62 web site: http://na62.web.cern.ch/NA62/Home/Home.html.

[2] J. Brod, M. Gorbahn and E. Stamou, *Two-loop electroweak corrections for the $K \to \pi\nu\bar{\nu}$ decays*, *Phys. Rev.* **D 83** (2011) 034030.

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[3] BNL E949 collaboration, S. Adler et al., *Measurement of the $K^+ \to \pi^+ \nu\bar{\nu}$*, *Phys. Rev.* **D 77** (2008) 052003.

[4] Timing, Trigger and Control (TTC) web site: http://ttc.web.cern.ch/TTC/intro.html.

[5] G. Haefeli et al., *The LHCb DAQ interface board TELL1*, *Nucl. Instrum. Meth.* **A 560** (2006) 494.

[6] NA62 collaboration, Technical Design Document: http://na62.web.cern.ch/NA62/Documents/TechnicalDesign.html.

[7] J. Christiansen et al., *Receiver ASIC for timing, trigger and control distribution in LHC experiments*, *IEEE Trans. Nucl. Sci.* **43** (1996) 1773 [INSPIRE].

[8] M. Mota et al., *A flexible multi-channel high-resolution time-to-digital converter ASIC*, *Proceedings of IEEE Nuclear Science Symposium 2000*, Lyon France (2000).

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