A 9-Channel, 100 ps LSB Time-to-Digital Converter for the NA62 Gigatracker Readout ASIC (TDCpix)

2012 JINST 7 C01065

(http://iopscience.iop.org/1748-0221/7/01/C01065)

PUBLISHED BY IOP PUBLISHING FOR SISSA

RECEIVED: *November 15, 2011*
ACCEPTED: *December 21, 2011*
PUBLISHED: *January 18, 2012*

TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2011,
26–30 SEPTEMBER 2011,
VIENNA, AUSTRIA

A 9-Channel, 100 ps LSB Time-to-Digital Converter for the NA62 Gigatracker Readout ASIC (TDCpix)

L. Perktold,[a,1] **G. Aglieri Rinella,**[a] **E. Martin,**[b] **M. Noy,**[a] **A. Kluge,**[a] **K. Kloukinas,**[a] **J. Kaplon,**[a] **P. Jarron,**[a] **M. Morel**[a] **and M. Fiorini**[a]

[a] *CERN,*
CH-1211 Geneva23, Switzerland
[b] *Universite Catholique de Louvain,*
1348 Louvain-la-Neuve, Belgium

E-mail: lukas.perktold@cern.ch

ABSTRACT: The TDCpix ASIC is the readout chip for the Gigatracker station of the NA62 experiment. Each station of the Gigatracker needs to provide time stamping of individual particles to 200 ps-rms or better. Bump-bonded to the pixel sensor the ASIC serves an array of 40 columns *x* 40 pixels. The high precision time measurement of the discriminated hit signals is accomplished with a set of 40 TDCs sitting in the End-Of-Column region of the ASIC. Each TDC provides 9 channels per column. For the time-to-digital converter (TDC) a delay-locked-loop (DLL) approach is employed to achieve a constant time binning of 100 ps. Simulation results show that an average rms time resolution of 33 ps with a power consumption of the TDC better than 33 mW per column is achieved. This contribution will present the design, simulation results and implementation challenges of the TDC.

KEYWORDS: Instrumentation for radioactive beams (fragmentation devices; fragment and isotope, separators incl. ISOL; isobar separators; ion and atom traps; weak-beam diagnostics; radioactive-beam ion sources); Pixelated detectors and associated VLSI electronics; Particle tracking detectors (Solid-state detectors)

[1] Corresponding author.

doi:10.1088/1748-0221/7/01/C01065

Contents

1 Introduction

The NA62 experiment [1] aims to measure the ultra rare $K^+ \to \pi^+ \nu\bar{\nu}$ decay at the SPS at CERN. Within the scope of the NA62 experiment the Gigatracker detector is responsible for providing precise angular, momentum and time measurement of the beam particles. Three independent Gigatracker stations are distributed along the beam to perform the measurements.

The Gigatracker station is a hybrid pixel detector composed of a planar sensor pump bonded to an array of 10 identical readout ASICs, referred to as the TDCpix. A sketch of one station with its 10 readout ASICs as well as the beam intensity profile across the setup is shown in figure 1.

A full-sized readout ASIC — the TDCpix — is currently under development [2]. Figure 2 shows a floorplan of the TDCpix ASIC with indications of the dimensions of the various blocks. Each of the TDCpix ASICs contains 1800 pixels arranged in a 40x45 matrix whereby each pixel has a size of 300 μm x 300 μm.

Whenever a charged particle is crossing the detector a signal is induced in the analog front end of the respective pixel. The analog front end is responsible for amplifying, shaping and discriminating the signal in amplitude and sending the hit over designated transmission lines to the End-Of-Column (EoC) region. The biases for the pixels are sitting in the EoC region.

For each pixel column a TDC performs the high-precision time measurement of the signals. Given the average rate of 58 k particles crossing the ASIC a total of 6.3 GBit/s of data is generated. A set of four 2.4 GBit/s serializers are employed to send the generated data off chip.

Each of the three Gigtracker station requires a time resolution better than 200 ps-rms. The overall timing uncertainty is represented by the timing uncertainty of the detector, the analog front-end as well as the TDC. To limit the contribution of the TDC to the overall time resolution, the TDC itself is required to provide a time resolution better than 60 ps-rms. The integration of high activity digital logic together with high precision analog blocks on the same substrate requires special attention not to degrade the overall time resolution of the system.

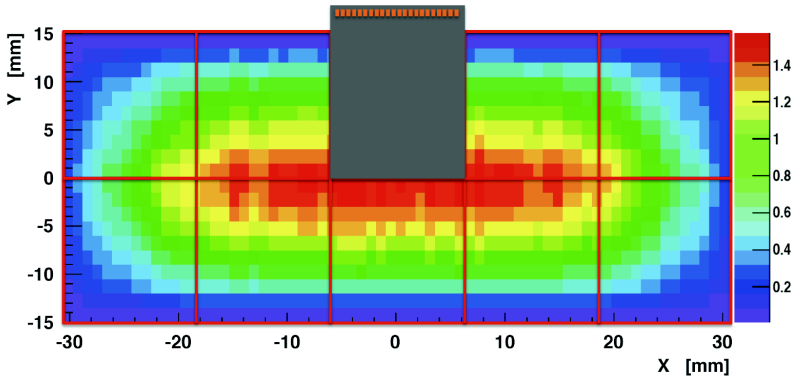

Figure 1. Arrangement of the readout ASICs of one Gigatracker station. The beam intensity profile is given in MHz/mm^2.

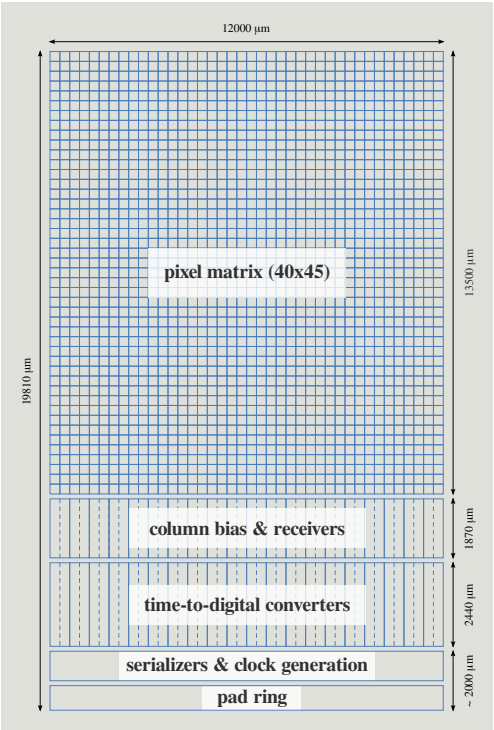

Figure 2. TCPpix top level block arrangement.

To be compatible with the pixel size, circuits common to all the columns are required to fit into a 300 μm frame. The maximum die-size of the ASIC is determined by the constraints set by the production and is not allowed to exceed a height of 21 mm. Additionally, due to the final arrangement of the Gigatracker station the ASIC can only be accessed from one of the short sides of the chip. This makes the routing of global signals and the distribution of power a challenging task.

The operating temperature of the stations needs to be below 5 °C to minimize the effects of the high radiation dose on the sensor. The deep sub-micron technology in use (130 nm) intrinsically reduces performance degradation of the ASIC due to total dose effects. Only circuits sensitive

2012 JINST 7 C01065

Table 1. TDCpix and TDC specifications.

Technology	130 nm (IBM)
Pixel size	300 μm *x* 300 μm
Maximum die size	12 mm *x* 21 mm
Average particle rate per pixel	58 kHz
Maximum operating temperature	5 °C
Nominal supply voltage	1.2 V
TDC: Maximum physical size	300 μm *x* 2.5 mm
TDC: Maximum power consumption	50 mW
TDC: Maximum time uncertainty (rms)	60 ps-rms

to voltage threshold shifts need to respect minor additional design rules [3]. To minimize the risk of single-event-upsets (SEUs), redundancy by triplicating the logic is applied throughout the ASIC. The maximum power of the ASIC is limited by the cooling requirements of the ASIC to 2 W/cm^2 [4]. For the TDC a maximum power budget of 50 mW is available.

As a proof of concept of the proposed architecture, a prototype chip with a single pixel column was produced and extensively tested as reported in [5] and [6]. The total power-consumption of the demonstrator TDC as well as its layout was not compatible with a full-sized implementation. This paper will concentrate on the critical aspects of the optimization of the TDC. Table 1 summarizes the specifications of the TDCpix ASIC and the specifications of the TDC.

2 The TDC of the TDCpix

A block diagram of the implemented architecture of the TDC is shown in figure 3. The TDC receives the 45 discriminated outputs of the pixels in one column. To share resources a set of 9 hit arbiters is responsible for multiplexing the hit signal from a group of 5 pixels. The TDC performs a Time-Over-Threshold (TOT) measurement of the received hit signals. Thereby, the rising and the falling edge of the hit are extracted by the hit arbiter units and sent to 9 channels of the TDC. Each channel of the TDC contains a separate set of registers for the rising and falling edge time measurement. To allow both a high time resolution and the measurement of large time differences a multistage approach has been followed. In a first stage completed clock cycles are counted whereas in a second stage a delay-locked-loop (DLL) is responsible for dividing the coarse counter clock period into smaller bins. The first stage is referred to as the coarse-time resolution block whereas the DLL is referred to as the fine-time resolution block. The hit leading and trailing edges trigger the latching of the coarse code counter and of the DLL fine-time code in the corresponding registers. For each hit the pixel address in a group as well as the coarse- and fine-resolution code are fetched and transferred to the pixel group FIFO. Data of different pixel groups are then multiplexed to the column FIFO. The whole data-flow is fully event driven, triggered by the hit.

To decouple the resolution of the DLL from the read out clock setting, the counter and the DLL are running on their separate clock domain. The configuration and monitoring of the blocks is accomplished with a custom serial interface (not shown in figure 3).

2012 JINST 7 C01065

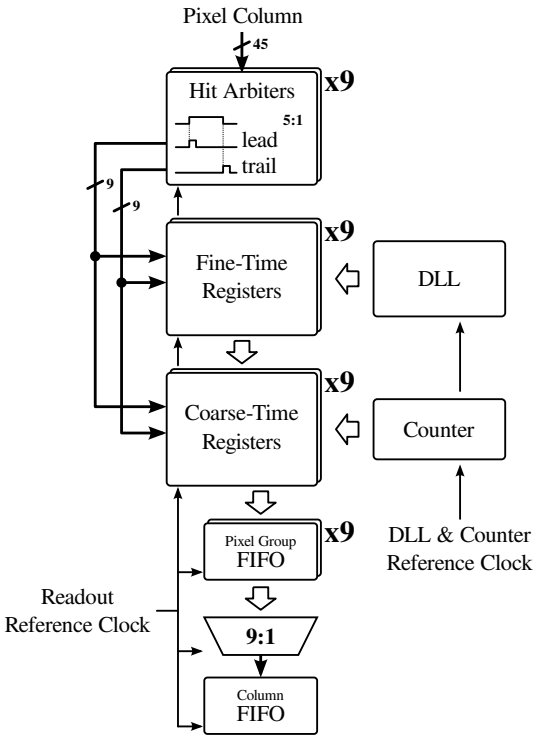

Figure 3. TDC architecture of the TDCpix readout ASIC.

2.1 Fine-time resolution block

In a DLL the phase of the input and the phase of the last output of the DLL are compared to continuously adjust the control voltage of the delay element to keep them equal. Employing a DLL instead of a plain delay line assures a constant bin-size across process-voltage-temperature (PVT) variations.

As shown in the block diagram of figure 4 there are 32 delay elements in the delay line. Assuming an input clock frequency of 320 MHz a bin-size of 97.7 ps is achieved. The exact delay of the elements is defined by the voltage stored on the loop filter capacitor (LF) and the setting of the minimum bias current. Depending on the region of operation the minimum bias current (min. Bias) can be set to limit the gain of the delay element.

To reduce the noise sensitivity of the DLL the delay line has been implemented in a fully differential manner using a Maneatis delay cell [7]. The single ended input clock of the DLL is converted to differential by using a single-ended to differential converter (SE/DE) at the input of the delay line. Distribution of the fine-time code is accomplished in a single ended manner by employing single-ended to differential converters (SE/DE) at the outputs of the DLL to save power. Distributing the fine-time code in a single ended manner is feasible since the propagation delay of high output codes of the DLL is much larger compared to the propagation delay due to the distribution. Equal bin sizes of the DLL are assured by placing dummy elements in front and behind the delay line as well as by placing dummy buffers at the output of the DLL. The inputs of the phase detector (PD) are tapped from the zeroth and 32nd output of the delay line. To close the loop a bang-bang phase detector in conjunction with a charge pump (CP) is used. To read out the

2012 JINST 7 C01065

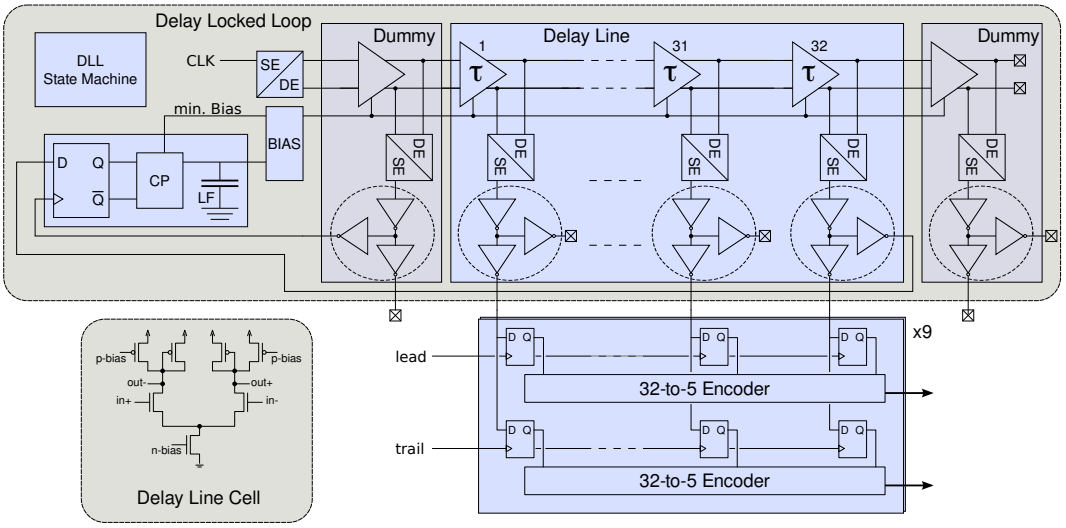

Figure 4. Fine-time resolution block diagram.

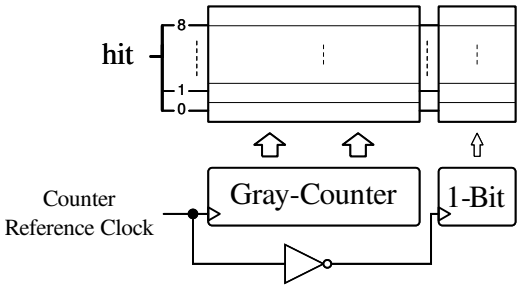

Figure 5. Synchronization scheme between the coarse counter and the DLL.

latched state of the DLL with a reasonable amount of signal routing a 32-to-5 bit encoder is locally added to the leading and trailing edge registers of each channel.

A state machine implemented with synthesized logic is responsible for controlling the start-up of the DLL and monitoring the state of the DLL during operation. The state machine also controls the setting of the charge pump current as well as the minimum bias current. It also provides access to the user to force the voltage on the feedback capacitor to any voltage value within the supply voltage range.

2.2 Synchronization among different domains

Upon the asynchronous arrival of the hit, the value of the coarse-time counter and of the DLL are stored in the TDC registers. When latching the state of the coarse counter an ambiguity might occur if the hit arrives during a code transition. This ambiguity can be resolved by employing a gray-code counter and using an additional bit clocked on the negative edge of the clock as depicted in figure 5. By looking at the fine-time code of the DLL in conjunction with the additional bit the ambiguity can be resolved. This scheme is efficient in terms of data volume since only one additional bit is needed to resolve the ambiguity.

2012 JINST 7 C01065

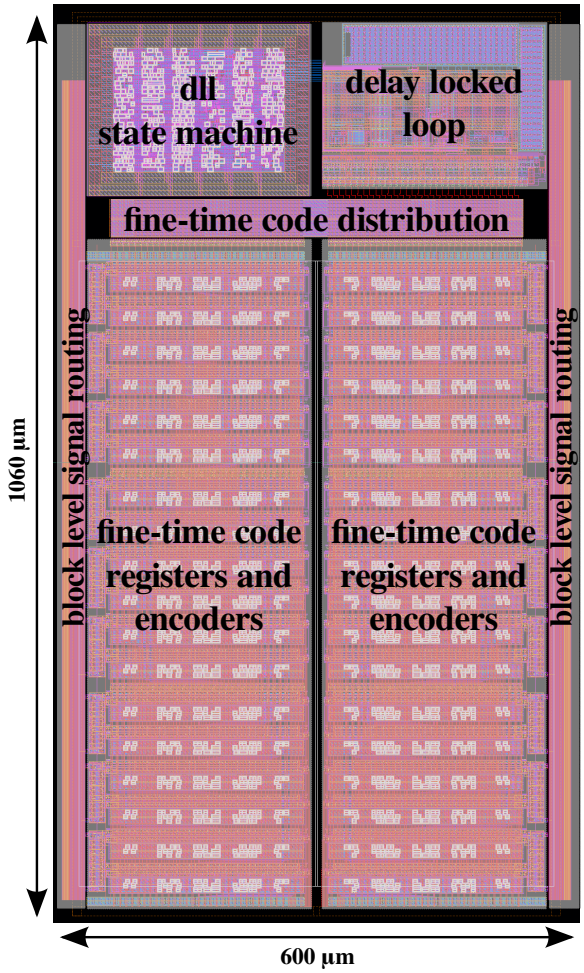

Figure 6. Floorplan of the fine-time resolution block.

The asynchronous arrival of the hit also requires a synchronization of the hit with respect to the readout clock. The synchronized hit signal is generated by the hit arbiter. This signal is synchronous with the readout clock and lasts at least for one complete clock cycle. This allows the time stamp registers to settle for at least one complete clock cycle before their data are copied to the readout FIFOs.

2.3 Physical integration

To simplify the routing problem one coarse counter is implemented per TDC and shared among the 9 channels. The DLL is shared among two adjacent columns to share resources. An image of the layout of the fine-time resolution block is shown in figure 6. Compared to a design with one DLL per column, sharing the DLL allows a reduction in power consumption of the fine-time resolution block by 18 % and reduces its area by 12%.

Sharing the DLL among two columns requires a careful design of a fully symmetric distribution network to fan out the fine-time code to the two banks of channels. Buffers are employed to reconstruct the signals to avoid degradation of slew time as the signals travel down the lines to

2012 JINST 7 C01065

Table 2. Key performance figures of the design (nominally operated at -20 °C,1.2 V and 320 MHz).

Figure	Nominally	Worst case	Specification
Area (per column)	300 μm x 2440 μm	-	300 μm x 2500 μm
Power consumption (per column)	33 mW	41 mW	$<$ 50 mW
Time resolution	33 ps-rms	51 ps-rms	$<$ 60 ps-rms

the registers. The distribution of hit lines traveling from the hit arbiter to their respective channels represents another critical aspect of the design. Due to the restricted area for block level signal routing the hits need to be distributed with minimum width lines routed next to each other at minimum distance. However, given the rate of hits on two adjacent lines and keeping the risetime of the signals below 200 ps only about 10^{-4} of the hits are expected to suffer from crosstalk.

To reduce noise coupling into the fine-time block of the TDC a separate dedicated power domain is employed. High resistive substrate trenches are used to isolate the substrates of the domains. The fine time code as well as the outputs of the channels need to be routed vertically across the hit registers. No routing space is available to route signals of the channels on the left and right side of the column since it is reserved for block level signal routing. The routing space for power distribution stripes is limited. Consequently, the power distribution has been carefully dimensioned to avoid any notable power supply drop.

3 Qualification, performance and testing

To qualify the various components of the TDC design, an extensive set of simulations has been carried out. Spectre and monte-carlo simulations have been run to verify the design of the DLL. Correct integration into the digital domain was verified by mixed-mode simulations. For the digital part an extensive verification using realistic hit stimuli was carried out. A top level test bench to verify the complete TDC is currently under development. The TDC is to be nominally operated at -20 °C with a 1.2 V power supply voltage and running at 320 MHz. For flexibility the range of operation was specified to be within $-20\,^{\circ}\mathrm{C} < 100\,^{\circ}\mathrm{C}$, $1.14\,V < 1.32\,V$ and $240\,\mathrm{MHz} < 320\,\mathrm{MHz}$. Table 2 lists key performance figures of the design.

Area: not only the width of the layout is a critical parameter but also the total height of each component sitting in the EoC area. In total only 6.5 mm are available below the pixel matrix. Together the column bias and the receivers extend 1.9 mm in height. The TDC itself fits in a 300 μm $\times$ 2440 μm frame. The hit arbiters consume 7 % of the area of the TDC, the fine-time resolution block 44 % and 49 % is occupied by the digital logic and the readout. In total the TDC occupies an area of 0.73 mm^2.

Power: as depicted in figure 7 the power consumption of the TDC is roughly equally shared among the fine-time resolution block and coarse-time resolution block with its digital logic included. In total the TDC consumes 33 mW per column which relates to a total of 1.3 W per chip.

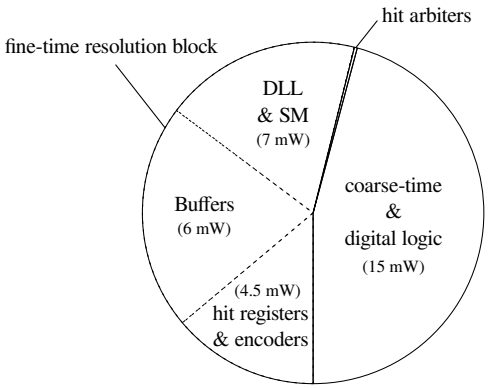

Figure 7. Power consumption contribution of the various blocks of the TDC.

Table 3. Expected rms-time resolution for different operating conditions.

Frequency	-20 °C, 1.14 V	27 °, 1.20 V	100 °, 1.32 V
240 MHz	44 ps (+ 7 ps)	42 ps (+ 5 ps)	41 ps (+ 4 ps)
320 MHz	33 ps (+ 5 ps)	32 ps (+ 3 ps)	31 ps (+ 3 ps)
480 MHz	23 ps (+ 2 ps)	22 ps (+ 2 ps)	22 ps (+ 1 ps)

An increase of up to 23% in power consumption is to be expected within the specified range of operation. This change is dominated by the quadratic dependence on supply voltage. The power consumption scales linearly, within a few percent, with frequency.

Noise: noise coupling into the time critical part of the TDC is too complex to be simulated in a reasonable time. The noise picked up by the time critical part of the TDC was measured on a demonstrator ASIC to be below 10 ps-rms. Due to space constraints the registers of the fine-time code resolution block and encoders share the same power domain. On chip decoupling MOS capacitance has been added to reduce the peak deviation on the supply voltage, caused by the activity of the circuits on the arrival of a hit, below 50 mV. A change in supply voltage translates in a change of delay in the DLL cells. The transfer coefficient was determined to be below 100 ps/V. Therefore, a negligible variation of 0.5 ps is to be expected due to supply voltage ripple.

Resolution: Monte-Carlo simulations have shown that the non-linearity error of the TDC under nominal conditions shows a DNL of 15 ps $\pm$ 8 ps and an INL of 13 ps $\pm$ 9 ps. Under worst case conditions the DNL increases up to 23 ps $\pm$ 15 ps and the INL up to 20 ps $\pm$ 13 ps. Reducing the DLL's clock frequency causes a degradation in time resolution due to bigger bin sizes of the TDC. Additionally, the matching among the cells in the DLL degrades with lower clock frequency. Table 3 lists the expected TDC time-resolution including its degradation due to 3σ variations of operating conditions. The listing includes the quantization error, the non-linearity contributions of the TDC as well as a noise-estimate of 10 ps-rms added in quadrature. If the INL of the TDC gets corrected offline the time-resolution of the TDC can be improved by up to 23%.

For a bang-bang DLL the phase detector should change its state each clock cycle. Thereby, the loop bandwidth of the DLL defines the excursion of the voltage ripple seen on the loop filter

2012 JINST 7 C01065

capacitance. Preferably, this ripple should be kept small to avoid a big change in delay of the delay elements. If the loop bandwidth is sufficiently small, the ripple on the loop filter capacitance can be reduced and will be limited by the hysteresis of the phase detector. When running at nominal frequency of 320 MHz, up to 6 cycles can be necessary before the phase detector switches. This relates to a change in delay of 0.28 ps per cell. Occasionally this can lead to the presence of two transitions in the latched DLL output code. The encoder circuit has been designed to cope with this situation.

The buffers to distribute the fine-time code of the TDC experience a +17 ps change in time-offset due to a -5 °C to 35 °C change in temperature. Over the specified range of supply voltages (ΔV=180 mV) a change in time offset of -76 ps is to be expected. Measurement results have shown that the front-end exhibits a 100 ps variation over the same range of temperatures [8]. Due to the relatively small variations compared to the front end electronics no mechanism to adapt the delay of the buffers on voltage and temperature variations is implemented.

For debugging purposes the TDC allows to read out the un-encoded data of the fine-time registers as well as to monitor the output of the phase detector of the DLL. Additionally, scan chains are implemented to allow testing of the digital portions of the design.

4 Conclusion

This paper presented the design challenges, the implementation and simulation results of the TDC for the TDCpix ASIC. Extensive verification demonstrates that the design fulfills the requirements set by the experiment. Including block level wiring the layout of the TDC fits in a 300 μm $\times$ 2440 μm frame and occupies in total an area of 0.73 mm^2. Under nominal conditions, the implementation achieves a time resolution of 33 ps-rms with a power consumption of 33 mW per column. The TDC shows good linearity with a DNL of 17 ps $\pm$ 10 ps and an INL of 14 ps $\pm$ 3.1 ps. Correcting for the INL error offline the resolution can be increased up to 23 %. The noise sensitivity of the fine-resolution block of the TDC has been carefully evaluated and several countermeasures have been taken to minimize the amount of noise coupled into the sensitive parts of the TDC.

References

[1] NA62 collaboration, *NA62 technical design technical report CERN*, European Organization for Nuclear Research (2010).

[2] G.A. Rinella et al., *The TDCpix readout ASIC: a 75 ps resolution timing front-end for the Gigatracker of the NA62 experiment*, in *Technology and Instrumentation in Particle Physics 2011 (TIPP2011)*, June 9–14, Chicago, U.S.A. (2011).

[3] F. Faccio and G. Gervelli *Radiation-induced edge effects in deep submicron CMOS transistors*, *IEEE Trans. Nucl. Sci.* **52** (2005) 2413.

[4] M. Morel et al., *The electro-mechanical integration of the NA62 GigaTracker time tagging pixel detector*, 2010 *JINST* **5** C12023.

[5] M. Noy et al., *Characterisation of the NA62 GigaTracker end of column readout ASIC*, 2010 *JINST* **6** C01086.

[6] M. Noy et al., *Characterisation of the NA62 GigaTracker end of column demonstrator hybrid pixel detector*, in *Topical Workshop on Electronics for Particle Physics 2011*, September 26–30, Vienna, Austria (2011).

[7] J.G. Maneatis, *Low-jitter process-independent DLL and PLL based on self-biased techniques*, *IEEE J. Solid-St. Circ.* **31** (1996) 130.

[8] E. Martin et al., *The 5 ns peaking time transimpedance front end amplifier for the silicon pixel detector in the NA62 Gigatracker*, *IEEE Nucl. Sci. Symp. Conf. Rec.* (2009) 381.

2012 JINST 7 C01065